Colin Drewes

775-830-9714 | colindrewes@gmail.com | colindrewes.com | PO BOX 3733, Incline Village Nevada, 89450

Education

Stanford University — Stanford, CA
PhD Student, Computer Science (2022-) — *GPA: 4.0*

University of California San Diego — La Jolla, CA
Master of Science, Computer Science (2022) — *GPA: 3.9*

University of California San Diego — La Jolla, CA
Bachelor of Science, Computer Science, Magna Cum Laude (2018-2021) — *GPA: 3.9*
Minor, Mathematics

Incline High School — Incline High School, NV
Honors Diploma, Valedictorian (2014-2018) — *GPA: 5.565*

Theses

Masters of Science in Computer Science — 2022
Next Generation Cloud-FPGA Side-Channels — *Committee: (Advisor) Ryan Kastner, Dean Tullsen, Deian Stefan*

Research Experience

Researcher in Winstein Lab — Winter 2023 -
Stanford — *Stanford, CA*
- Working with Professor Keith Winstein on functional operating systems and distributed runtimes.

Researcher in Trippel Lab — Fall 2022 -
Stanford — *Stanford, CA*
- Working with Professor Caroline Trippel to build and verify heterogeneous memory consistency models.

Researcher in Kastner Lab — 2019 -
University of California San Diego — *La Jolla, CA*
- Lead research projects broadly exploring FPGA security in cloud environments. Advised undergraduates independently and through ERSP. Collaborated with other universities (University of Washington), and industry (Georgia Tech Research Institute). Received NSF Computer and Network Systems (CNS) fellowship and NSF Summer Research Fellowship.

Research Comparing Methods of Phylogenetic Reconstruction — 2016 - 2018
University of Nevada, Reno — *Reno, NV*
- Worked with Professor Guy Hoelzer from the University of Nevada, Reno on a comparison of different phylogenetic reconstruction methods (RAxML, FastTree and HPA) which resulted in a final self-directed paper

Work Experience

Software Engineering Intern — Summer 2022
Arista Networks — *Remote*
- Worked on the engineering production team, developing containerization and build orchestration software.

Security Research Intern — Summer/Fall 2020, Winter 2021
Georgia Tech Research Institute — *Remote*
- Researcher for the Cybersecurity, Information Protection, and Hardware Evaluation research group of the Georgia Tech Research Institute. My work focused on ensuring optimality of placement/routing of designs onto FPGAs.

Personal Research

Globally Irreversible Locally Reversible Winter 2022
University of California San Diego *La Jolla, CA*

- In this paper I present ideas on how reversible computing could be integrated into an existing CPU architecture. This lowers the barrier of adoption for reversible computing techniques, allowing for significant power savings without requiring new higher-level language paradigms .

A Reconfigurable RISC-V Co-Processor Fall 2021
University of California San Diego *La Jolla, CA*

- In this paper I present the design of a CPU utilizing an FPGA as co-processor with physical access to the registers as well as memory of the processor. I claim this architecture will have the following improvements over standard CPUs and existing CPU-FPGA hybrids: 1) ability to adjust at the hardware level to changing workloads at runtime, 2) less wasted silicon on specialized ASIC co-processors (crypto, vector operations...), 3) improved power efficiency, 4) and simplified compatibility with other ISA extensions and deprecated instructions.

Efficient, High Detail and Dynamic Julia Sets Winter 2021
University of California San Diego *La Jolla, CA*

- A tool for generating high resolution Julia sets efficiently.

Circle Hough Transform for Cell Detection Winter 2020
University of California San Diego *La Jolla, CA*

- A simple and effective python script for identifying cells within images in response to lacking commercial tools for comet assays (a measure of DNA damage).

How well does HPA perform against existing phylogenetic estimation methods? Winter 2018
Incline High School *Incline Village, NV*

- A self-directed research project comparing the accuracy of different phylogenetic reconstruction methods.

Teaching and Mentorship

Mentorship

- Advised computer science undergraduates participating in UCSD's Early Researchers Scholars Program

Teaching Assistant

- University of California San Diego, CSE 160: Intro to Parallel Computing, Winter 2022
- University of California San Diego, CSE 101: Design and Analysis of Algorithms, Fall 2021

Service

Additional Reviewer

- 2023 IEEE 31th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)
- 2022 IEEE 30th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)

Talks

Conference Talks

- *Turn on, Tune in, Listen up: Maximizing Channel Capacity in Time-to-Digital Converters* — ACM/SIGDA International Symposium on Field-Programmable Gate Arrays
- *Classifying Computations on Multi-Tenant FPGAs* — 58th Design and Automation Conference

Invited

- *Pentimento: Data Residue in Digital Hardware* — Workshop on the Security for Custom Computing Machines, 2023
- *At-tenant-uator: Isolating Power Side-Channels in Shared-FPGAs* — Workshop on the Security for Custom Computing Machines, 2022
- *Classifying Computations on Multi-Tenant FPGAs* — University of California, Santa Barbara, Arch Lab, 2021

Awards

Research

- International Symposium on Field Programmable Gate Arrays Best Paper Candidate
- UCSD CSE Department MS Excellence in Research Award, 2022
- NSF Computer and Network Systems fellowship under the auspices of Professor Ryan Kastner

Academic

- University of California San Diego Provost Honors, 2018-2021
- Valedictorian, 2018
- AP National Scholar and AP Capstone Scholar, 2018

Publications

Theses

- **Colin Drewes**, *Next Generation Cloud-FPGA Side-Channels*, MS Thesis, Department of Computer Science and Engineering, University of California San Diego, 2022.

Full Papers

- **Colin Drewes**, Olivia Weng, Andres Meza, Alric Althoff, David Kohlbrenner, Ryan Kastner, Dustin Richmond. *Pentimento: Data Residue in Cloud FPGAs.* In submission.
- **[Best Paper Candidate] Colin Drewes**, Olivia Weng, Keegan Ryan, William Hunter, Christopher McCarty, Ryan Kastner, Dustin Richmond. *Turn on, Tune in, Listen up: Maximizing Channel Capacity in Time-to-Digital Converters*, in 2023 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA).
- M. Gobulukoglu, **C. Drewes**, B. Hunter, R. Kastner, and D. Richmond, *Classifying Computations on Multi-Tenant FPGAs*, in Design Automation Conference (DAC), 2021.

Posters

- **C. Drewes**, S. Harris, W. Wang, R. Appen, O. Weng, R. Kastner, W. Hunter, C. McCarty, and D. Richmond, *A Tunable Dual-Edge Time-to-Digital Converter*, in International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2021, pp. 1-1.
- Mustafa Gobulukoglu, **Colin Drewes**, Bill Hunter, Dustin Richmond, and Ryan Kastner. 2021. *Classifying Computations on Multi-Tenant FPGAs.* In The 2021 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA '21). Association for Computing Machinery, New York, NY, USA, 227.