Turn on, Tune in, Listen up Maximizing Side-Channel Recovery in Time-to-Digital Converters

Colin Drewes¹, Olivia Weng¹, Keegan Ryan¹, Bill Hunter², Christopher McCarty², Ryan Kastner¹, and Dustin Richmond³

¹UCSD, ²GTRI, ³UCSC

February 13, 2023



FPGAs are powerful...but often prohibitively expensive This has pushed us towards...

This has pushed us towards...

Cloud-FPGA leasing schemes (temporal sharing)

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.



This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.

While logical boundaries may be in place, they all share the same power system!

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.

While logical boundaries may be in place, they all share the same power system!

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.

While logical boundaries may be in place, they all share the same power system!

If a dedicated actor were able to instantiate a voltage fluctuation sensor within their allocated logic they could...

Determine what core other actors are executing

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.

While logical boundaries may be in place, they all share the same power system!

- Determine what core other actors are executing
- Determine what is running on an actor's soft-processor

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.

While logical boundaries may be in place, they all share the same power system!

- Determine what core other actors are executing
- Determine what is running on an actor's soft-processor
- Perform a correlation power analysis attack

This has pushed us towards...

- Cloud-FPGA leasing schemes (temporal sharing)
- Integration of proprietary IP
- Full FPGA virtualization (temporospatial sharing)

Observation: These are all multi-actor structures—potentially running hidden opaque circuitry.

While logical boundaries may be in place, they all share the same power system!

- Determine what core other actors are executing
- Determine what is running on an actor's soft-processor
- Perform a correlation power analysis attack
- Detect round 7 of AES to introduce a power fault into the system



We refine our threat model around cloud multi-tenant FPGAs—but we study fundamental qualities of voltage fluctuation sensors that can apply to any multi-actor structure.

 Attacker co-locates with another user and deploys voltage sensor



- Attacker co-locates with another user and deploys voltage sensor
- 2. Collects sensor readings



- Attacker co-locates with another user and deploys voltage sensor
- 2. Collects sensor readings
- 3. Optimize θ and ϕ based on readings



- 1. Attacker co-locates with another user and deploys voltage sensor
- 2. Collects sensor readings
- 3. Optimize θ and ϕ based on readings
- 4. Extract data from sensor readings



We are interested in Time-to-Digital Converters (TDC):

We are interested in Time-to-Digital Converters (TDC):

1. An instrument for synchronously measuring the load on the power distribution network

We are interested in Time-to-Digital Converters (TDC):

- 1. An instrument for synchronously measuring the load on the power distribution network
- 2. Easy to disguise as they resemble carry-adders and can be designed to include no timing violations

We are interested in Time-to-Digital Converters (TDC):

- 1. An instrument for synchronously measuring the load on the power distribution network
- 2. Easy to disguise as they resemble carry-adders and can be designed to include no timing violations
- A brief overview of a canonical TDC.

We are interested in Time-to-Digital Converters (TDC):

- 1. An instrument for synchronously measuring the load on the power distribution network
- 2. Easy to disguise as they resemble carry-adders and can be designed to include no timing violations
- A brief overview of a canonical TDC.



*An array of elements with uniform delay

We are interested in Time-to-Digital Converters (TDC):

- 1. An instrument for synchronously measuring the load on the power distribution network
- 2. Easy to disguise as they resemble carry-adders and can be designed to include no timing violations

A brief overview of a canonical TDC.



*Launch clock sends rising/falling pulses through delay elements

We are interested in Time-to-Digital Converters (TDC):

- 1. An instrument for synchronously measuring the load on the power distribution network
- 2. Easy to disguise as they resemble carry-adders and can be designed to include no timing violations

A brief overview of a canonical TDC.



*Capture clock, which is phase offset a constant value from the launch, captures how far signals propagated through delay elements

We are interested in Time-to-Digital Converters (TDC):

- 1. An instrument for synchronously measuring the load on the power distribution network
- 2. Easy to disguise as they resemble carry-adders and can be designed to include no timing violations

A brief overview of a canonical TDC.



Capture output distance \propto state of the PDN

This is a nice theoretical model:



This is a nice theoretical model:



Perfect delay line doesn't exist:

This is a nice theoretical model:



Perfect delay line doesn't exist:

More linear propagation = more responsive to fluctuations

This is a nice theoretical model:



Perfect delay line doesn't exist:

- More linear propagation = more responsive to fluctuations
- Faster propagation = higher resolution

<ロト < 団ト < 団ト < 臣ト < 臣ト 王 の Q (C) 6/14

Map TDC to CARRY primitives. Fast and linear....locally.

Map TDC to CARRY primitives. Fast and linear....locally.



Map TDC to CARRY primitives. Fast and linear....locally.





Map TDC to CARRY primitives. Fast and linear....locally.



The data bears this out. Linear 4 bits on PYNQ (CARRY4s), linear 8 bits on AWS (CARRY8s).


Known Problems: Architectural Irregularities

Map TDC to CARRY primitives. Fast and linear....locally.



The data bears this out. Linear 4 bits on PYNQ (CARRY4s), linear 8 bits on AWS (CARRY8s).



6/14

Constant phase offset.



Dynamic phase offset.



Dynamic phase offset.



Leverage programmable clock generator

Dynamic phase offset.



- Leverage programmable clock generator
- Propagation distance is now configurable

Dynamic phase offset.



- Leverage programmable clock generator
- Propagation distance is now configurable
- Attacker can place transition at ideal point within CARRY primitive, improving sensor response to power fluctuations.

 θ, the phase relationship between launch and capture defines a window

- θ, the phase relationship between launch and capture defines a window
- Only power fluctuations within window are captured by the TDC

- θ, the phase relationship between launch and capture defines a window
- Only power fluctuations within window are captured by the TDC
- Victim core is also likely synchronous, and induced power fluctuation is brief

- θ, the phase relationship between launch and capture defines a window
- Only power fluctuations within window are captured by the TDC
- Victim core is also likely synchronous, and induced power fluctuation is brief





- θ, the phase relationship between launch and capture defines a window
- Only power fluctuations within window are captured by the TDC
- Victim core is also likely synchronous, and induced power fluctuation is brief

Bad Phase (ϕ) Alignment!



Good Phase (ϕ) Alignment!



- θ, the phase relationship between launch and capture defines a window
- Only power fluctuations within window are captured by the TDC
- Victim core is also likely synchronous, and induced power fluctuation is brief
- Lets phase shift launch and capture clock together, wrt victim computation

Bad Phase (ϕ) Alignment!



Good Phase (ϕ) Alignment!



< ロ > < 同 > < 回 > < 回 >

Our θ tunable Time-to-Digital Converter:



Our θ tunable Time-to-Digital Converter:



Our θ and ϕ tunable Time-to-Digital Converter:



 Instantiate sensor alongside soft-processor AES. Both 25MHz.

- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate φ by two periods with processor disabled and measure.

- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate φ by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.

- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate φ by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.

Expect to see a single optimal ϕ

- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate \u03c6 by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.



- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate \u03c6 by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.



- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate \u03c6 by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.



- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate \u03c6 by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.
- \blacktriangleright Background sweep varies by ϕ



・ ロ ト ・ 同 ト ・ 三 ト ・ 三 ト

10/14

- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate \u03c6 by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.
- Background sweep varies by ϕ
- Optimal \u03c6 blends into sensor background noise



・ ロ ト ・ 同 ト ・ 三 ト ・ 三 ト

10/14

- Instantiate sensor alongside soft-processor AES. Both 25MHz.
- Rotate \u03c6 by two periods with processor disabled and measure.
- Rotate \u03c6 by two periods with processor enabled and measure.
- Background sweep varies by ϕ
- Optimal \u03c6 blends into sensor background noise



Taking the difference from the background exposes optimal ϕ to capture power fluctuations induced by victim.

 Sensor co-located with each of 13 victim computations on multiple boards

- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ

- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ
- Sensor is sampled as victim executes

- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ
- Sensor is sampled as victim executes
- Some number of boards are reserved for training, some for testing, representing the hypothetical divide between cloud and local FPGAs.

- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ
- Sensor is sampled as victim executes
- Some number of boards are reserved for training, some for testing, representing the hypothetical divide between cloud and local FPGAs.
- The data is then processed....



- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ
- Sensor is sampled as victim executes
- Some number of boards are reserved for training, some for testing, representing the hypothetical divide between cloud and local FPGAs.
- The data is then processed....

	Raw Data	
1		
	Fast Fourier Transfor	m
2		-

- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ
- Sensor is sampled as victim executes
- Some number of boards are reserved for training, some for testing, representing the hypothetical divide between cloud and local FPGAs.
- The data is then processed....



- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ
- Sensor is sampled as victim executes
- Some number of boards are reserved for training, some for testing, representing the hypothetical divide between cloud and local FPGAs.
- The data is then processed....



- Sensor co-located with each of 13 victim computations on multiple boards
- Sensor is tuned to some value of θ and φ to minimize (maximize) θ and φ
- Sensor is sampled as victim executes
- Some number of boards are reserved for training, some for testing, representing the hypothetical divide between cloud and local FPGAs.
- The data is then processed....
- Classification accuracy across 13 applications reflects the sensors ability to capture sensitive information across the channel.



Classification Accuracy by Tuning Configuration

 Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).

Classification Accuracy by Tuning Configuration

Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).



Classification Accuracy by Tuning Configuration

- Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).
- Good θ: max standard deviation of θ, and min φ.


- Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).
- Good θ: max standard deviation of θ, and min φ.



- Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).
- Good θ: max standard deviation of θ, and min φ.
- Good θ and φ: max standard deviation of θ, and max φ.



- Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).
- Good θ: max standard deviation of θ, and min φ.
- Good θ and φ: max standard deviation of θ, and max φ.



- Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).
- Good θ: max standard deviation of θ, and min φ.
- Good θ and φ: max standard deviation of θ, and max φ.
- Good θ and φ: with φ
 background subtraction.



- Worst case: min standard deviation of θ (likely a plateau), and φ (likely phase misaligned).
- Good θ: max standard deviation of θ, and min φ.
- Good θ and φ: max standard deviation of θ, and max φ.
- Good θ and φ: with φ
 background subtraction.



Check the cross validation performance

 Test every combination and number of training and testing board

- Test every combination and number of training and testing board
- Examine accuracy vs # training boards. Reduces IQR by 2.3X.



- Test every combination and number of training and testing board
- Examine accuracy vs # training boards. Reduces IQR by 2.3X.
- Examine loss vs # training boards. Reduces IQR by 5.8X.



- Test every combination and number of training and testing board
- Examine accuracy vs # training boards. Reduces IQR by 2.3X.
- Examine loss vs # training boards. Reduces IQR by 5.8X.
- Data generalizes better



Check the cross validation performance

- Test every combination and number of training and testing board
- Examine accuracy vs # training boards. Reduces IQR by 2.3X.
- Examine loss vs # training boards. Reduces IQR by 5.8X.
- Data generalizes better



Background Subtraction is Out-of-Distribution Generalization!

Conclusion/Questions

