Pentimento

Data Residue in Digital Hardware

Colin Drewes[1], Olivia Weng[2], Andres Meza[2], Alric Althoff[3], David Kohlbrenner[4], Ryan Kastner[2], and Dustin Richmond[5]

[1]Stanford, [2]UCSD, [3]Cycuity, [4]UW, [5]UCSC

February 12, 2023

An Analogy

Pentimento—The presence or reemergence of early images which have since been painted over.

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Rembrandt's *An Old Man in Military Costume*

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Why?

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- Reusing canvases

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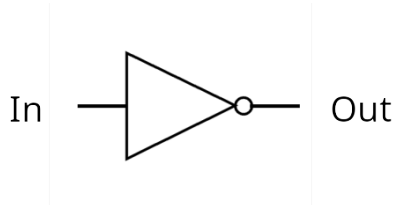
Idealized view of digital logic



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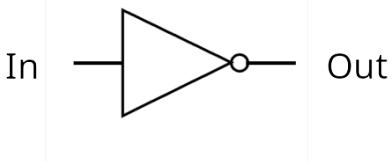

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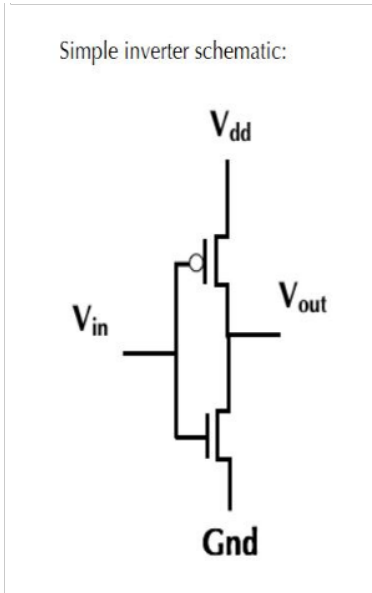

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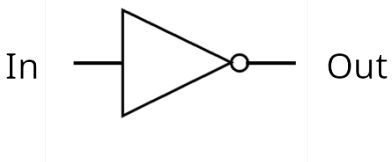

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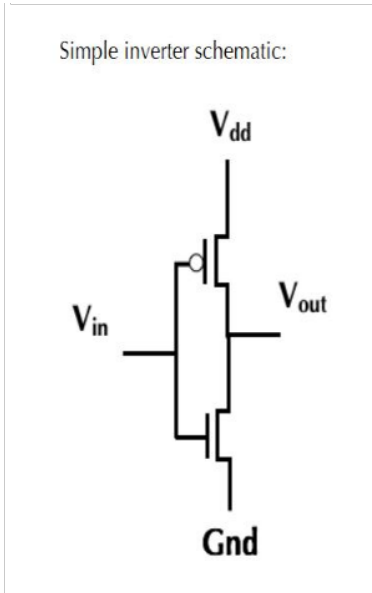

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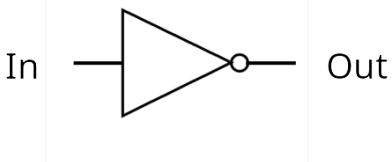

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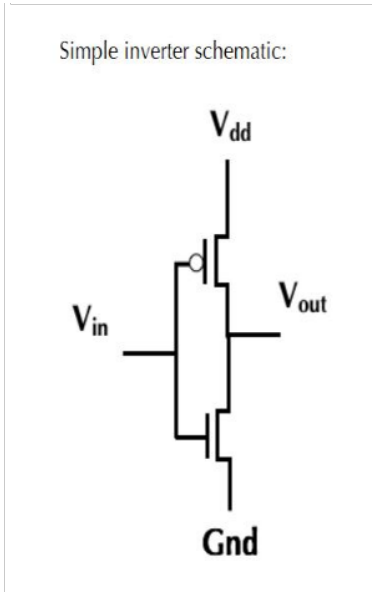

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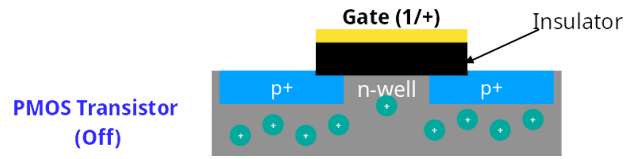

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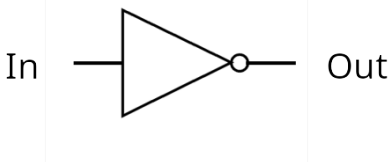

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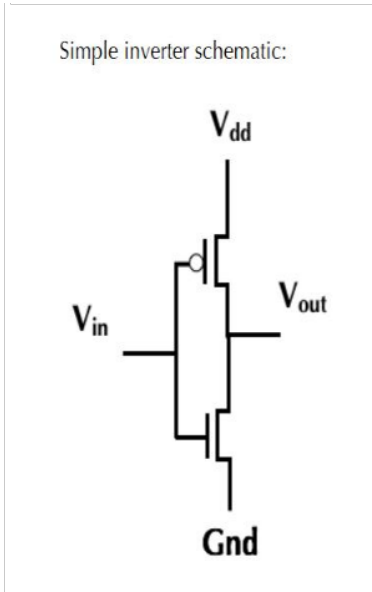

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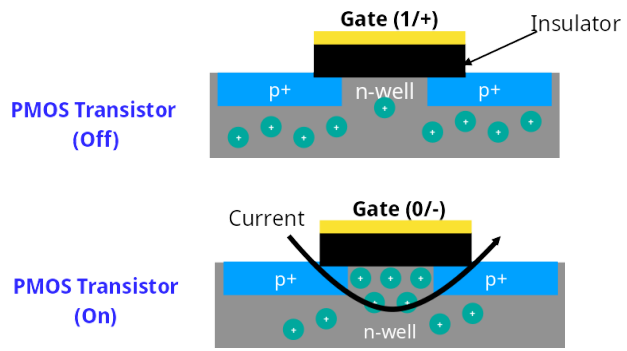

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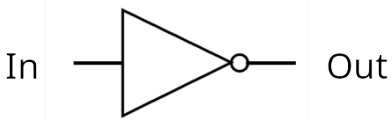

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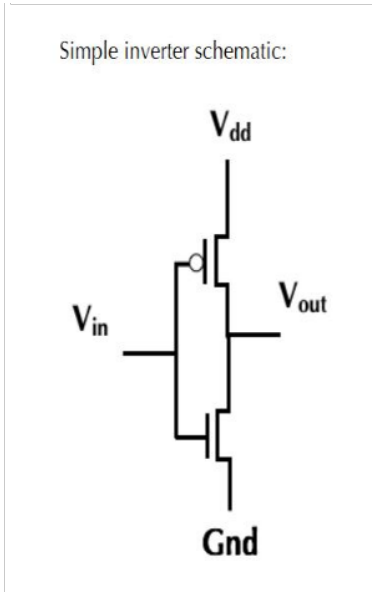

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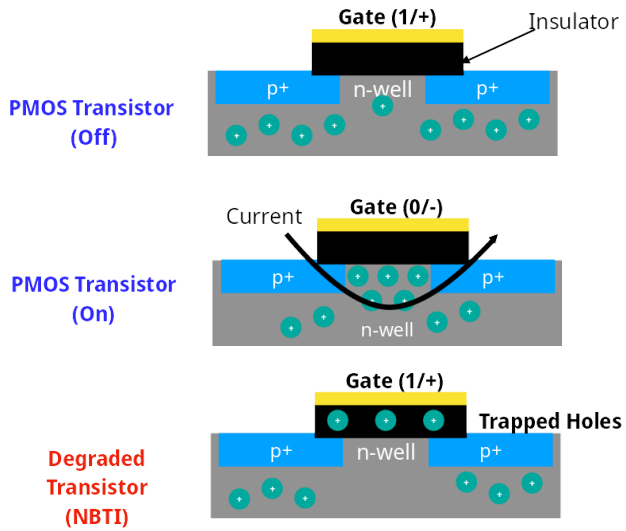
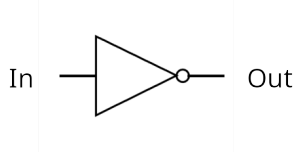


"Negative (-) Bias Temperature Instability"(a Pentimento?)

A Pentimenti Emerges



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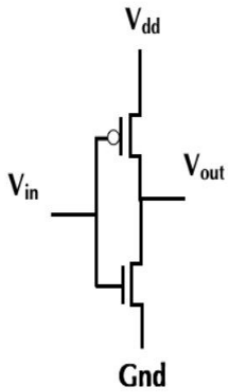

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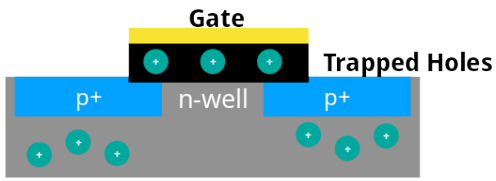
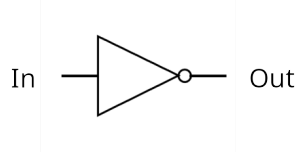


Degraded Transistor (NBTI)

"Negative (-) Bias Temperature Instability"



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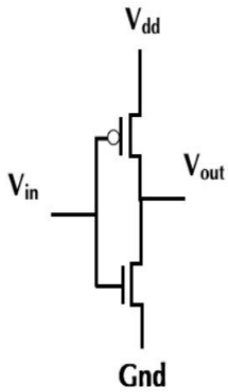

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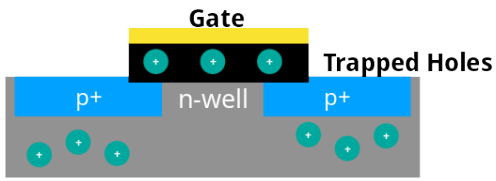

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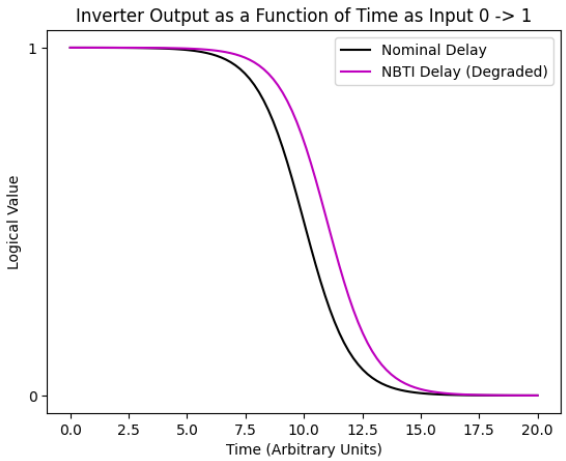

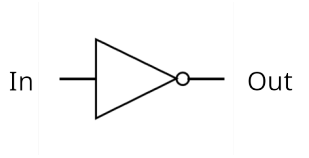

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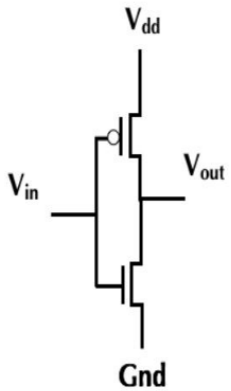

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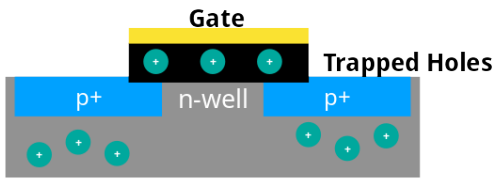

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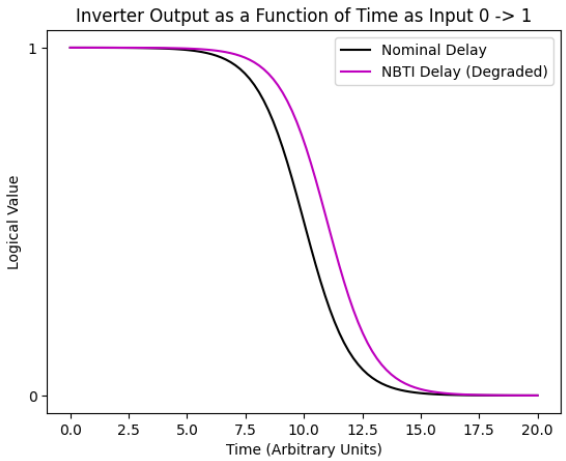

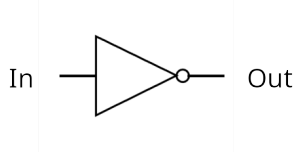

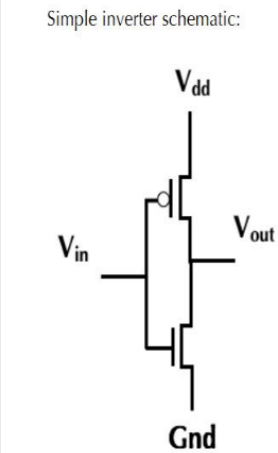

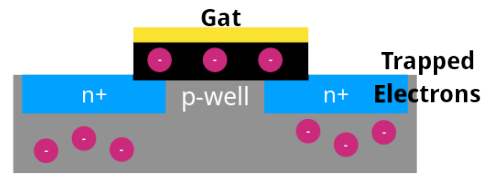

Degraded Transistor (PBTI)

"Positive Bias (+) Temperature Instability"

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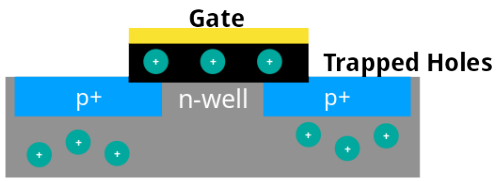

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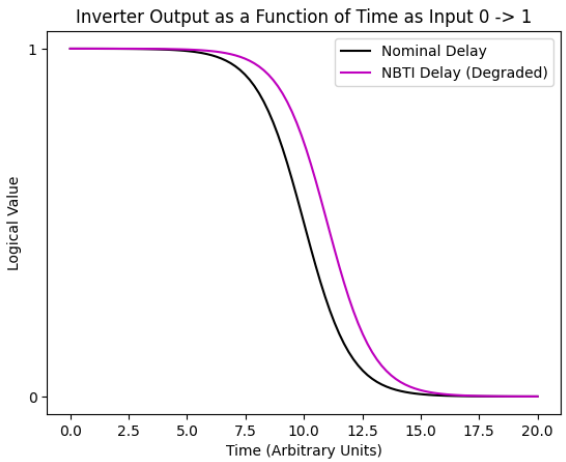

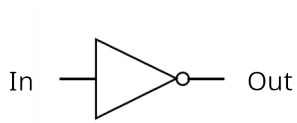

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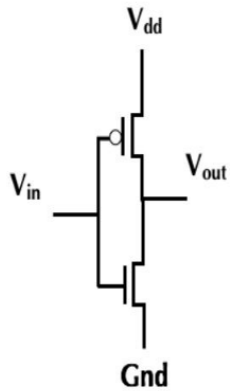

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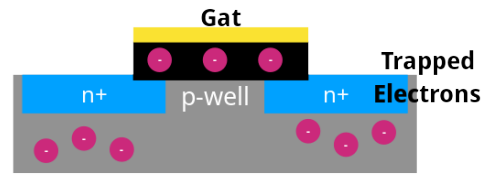

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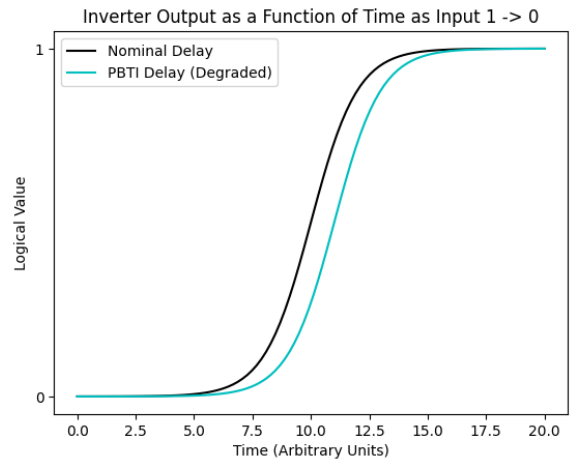

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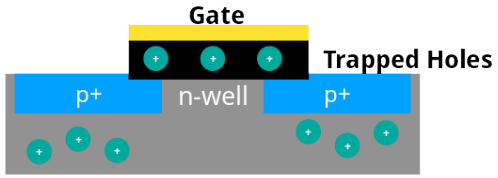
BTI effects create long term measurable timing differences—a pentimenti.



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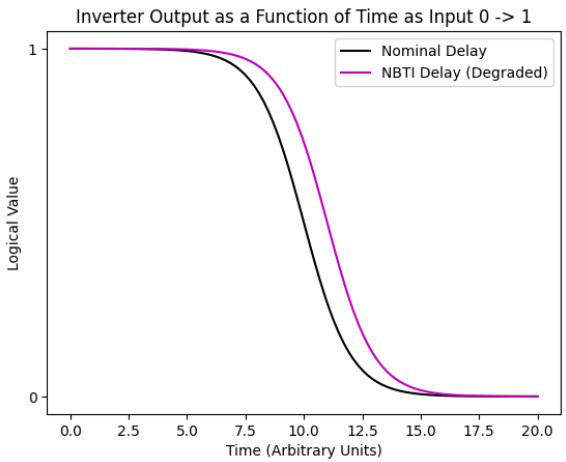

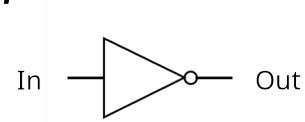

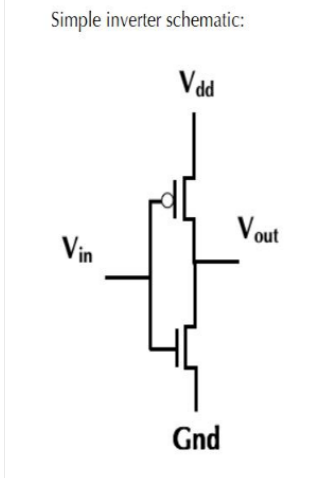

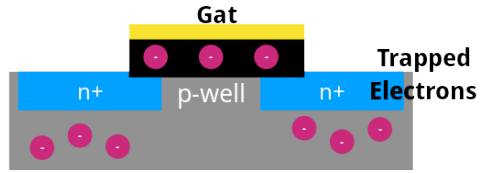

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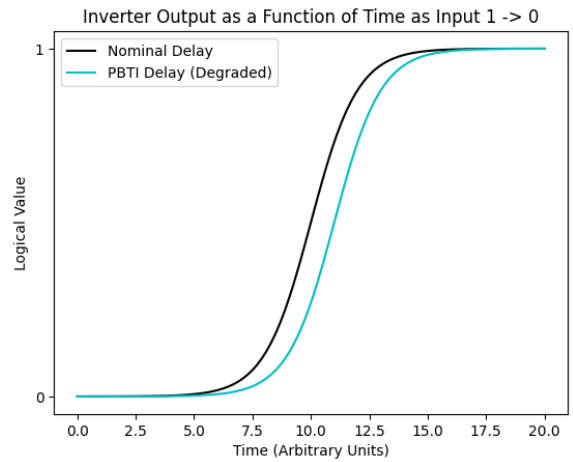

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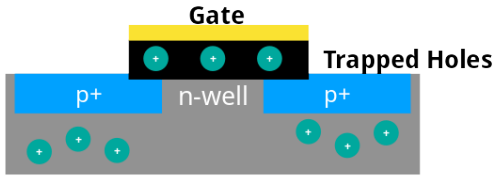

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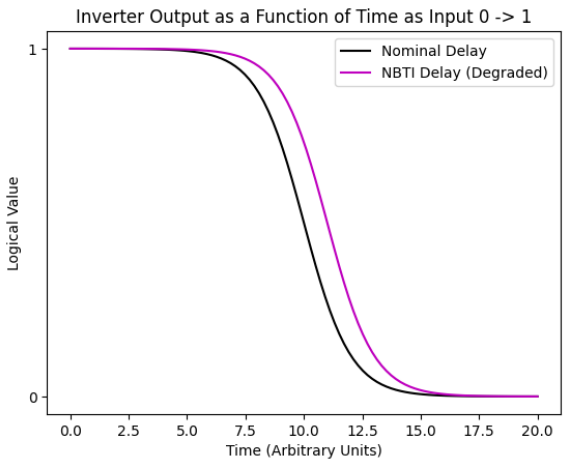

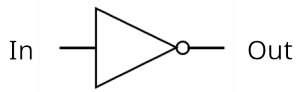

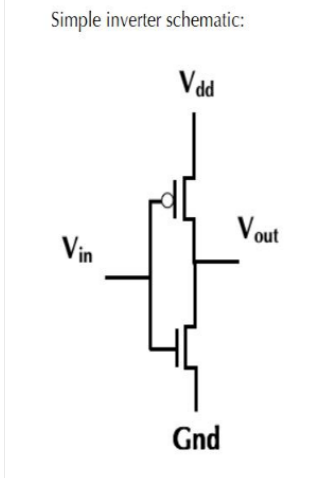

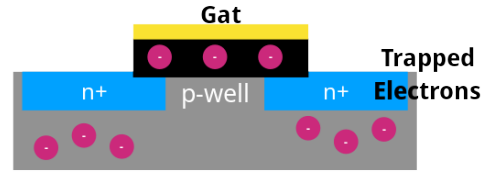

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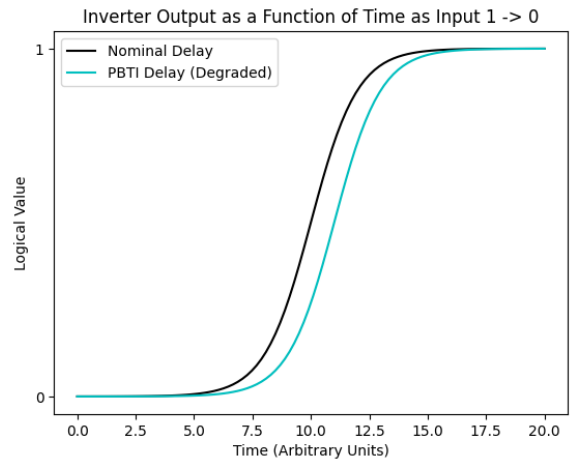

If we can precisely measure timing through digital components, we can determine the previous logical value they held.

A High-Risk Target

Cloud-Resident FPGAs

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- Consecutive users with the expectation of logical isolation.

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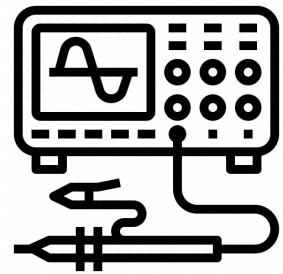
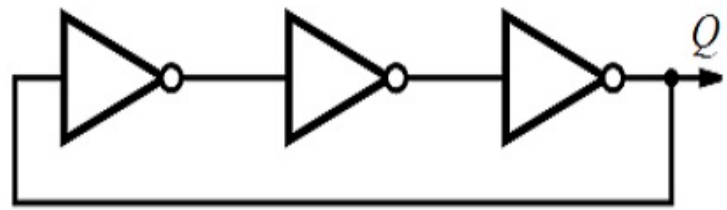
- BTI has been measured on local FPGAs using conventional means and with PL sensors.



Zick et al. FPL 2014.



Pfeifer et al. FPL 2013
Amouri et al, FPL 2014
Stott et al. FPGA 2010

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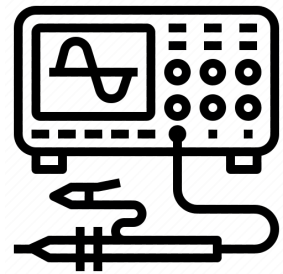
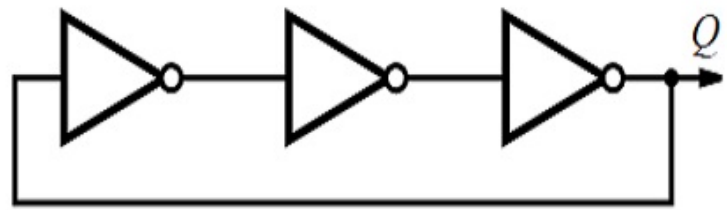


Zick et al. FPL 2014.

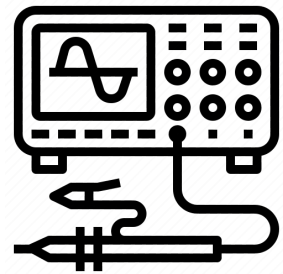


Pfeifer et al. FPL 2013
Amouri et al, FPL 2014
Stott et al. FPGA 2010

A High-Risk Target

Cloud-Resident FPGAs

- Consecutive users with the expectation of logical isolation.
- BTI has been measured on local FPGAs using conventional means and with PL sensors.
- PL sensors enable a remote attack.
- Never applied to the cloud. Most work focuses on reliability testing, or long term data remanence.



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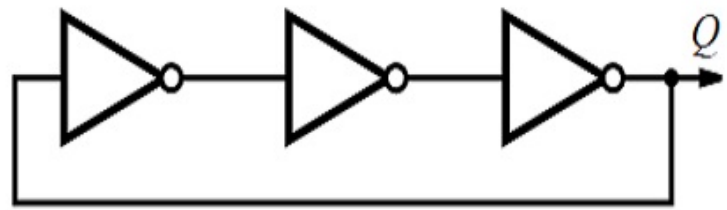

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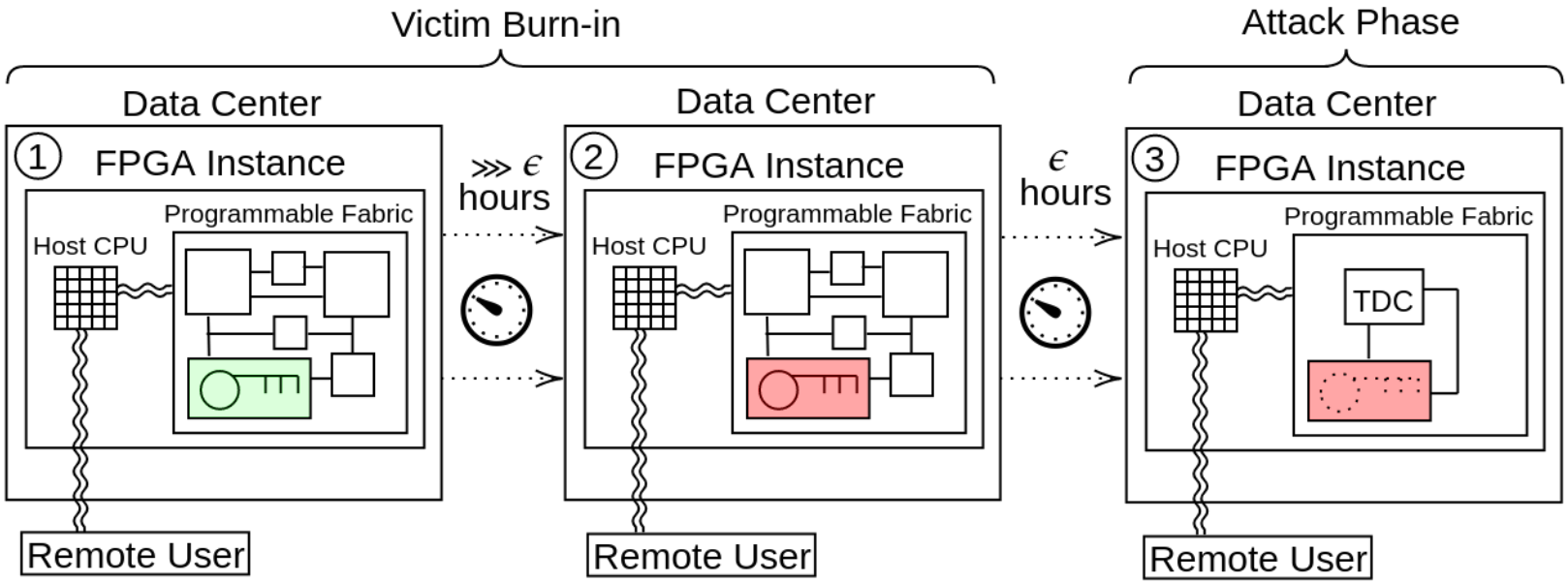
Our No-Contact, Legal Circuit, Threat Model



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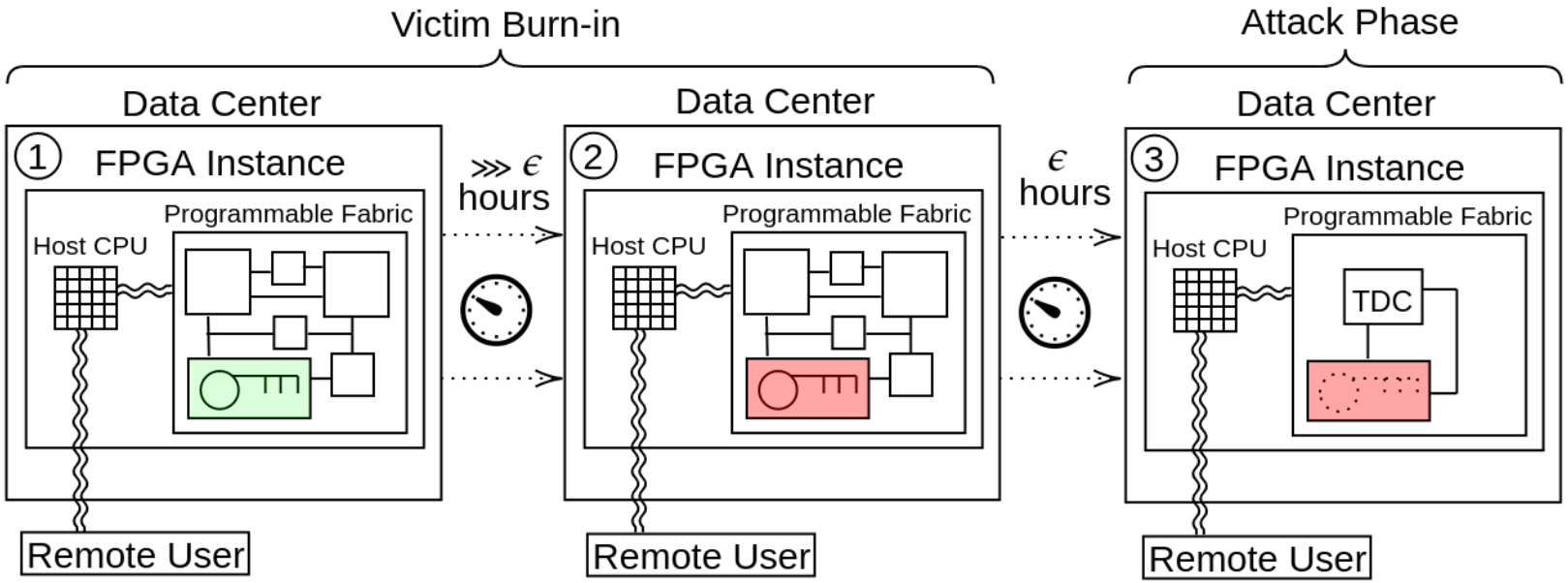

- User rents cloud-FPGA and performs computation using some sensitive data

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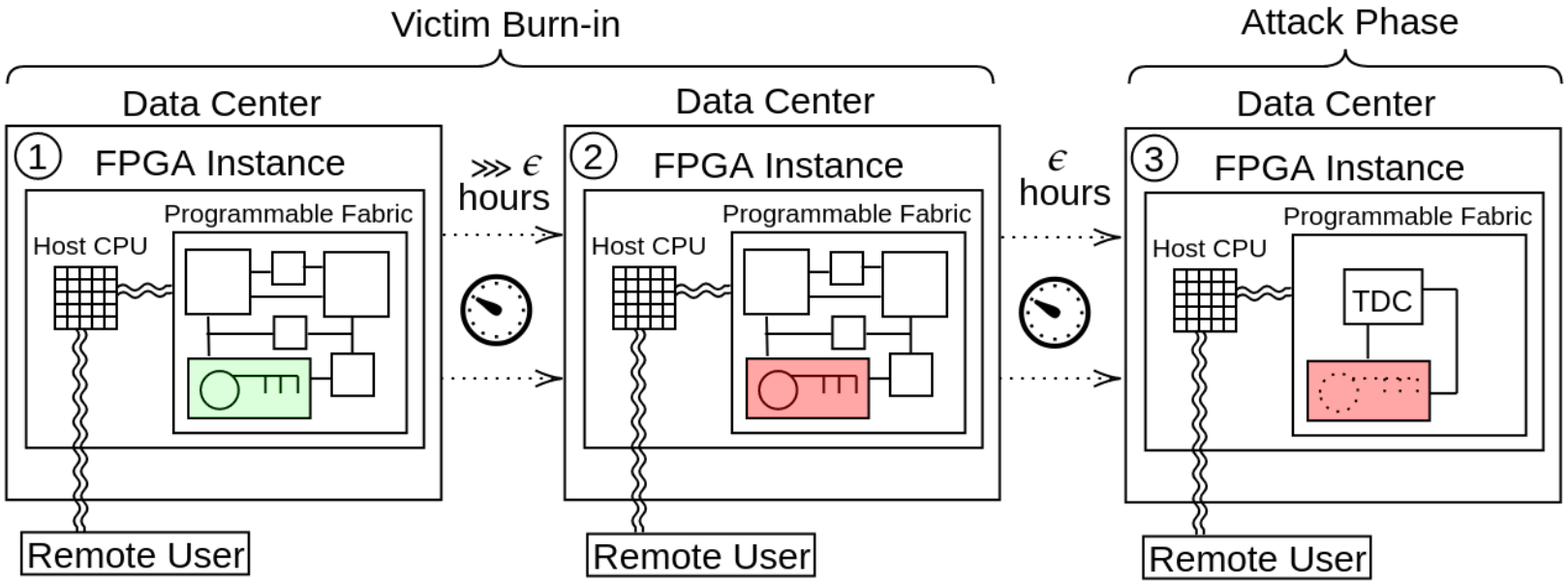

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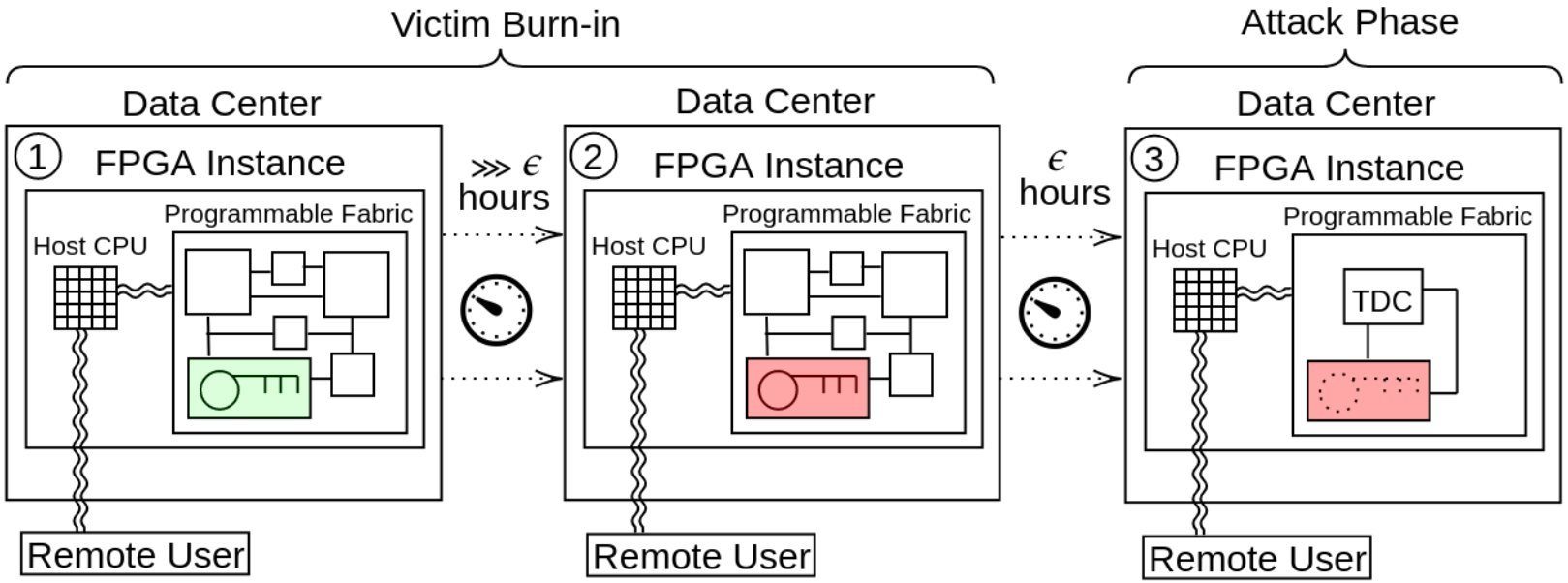

- User rents cloud-FPGA and performs computation using some sensitive data
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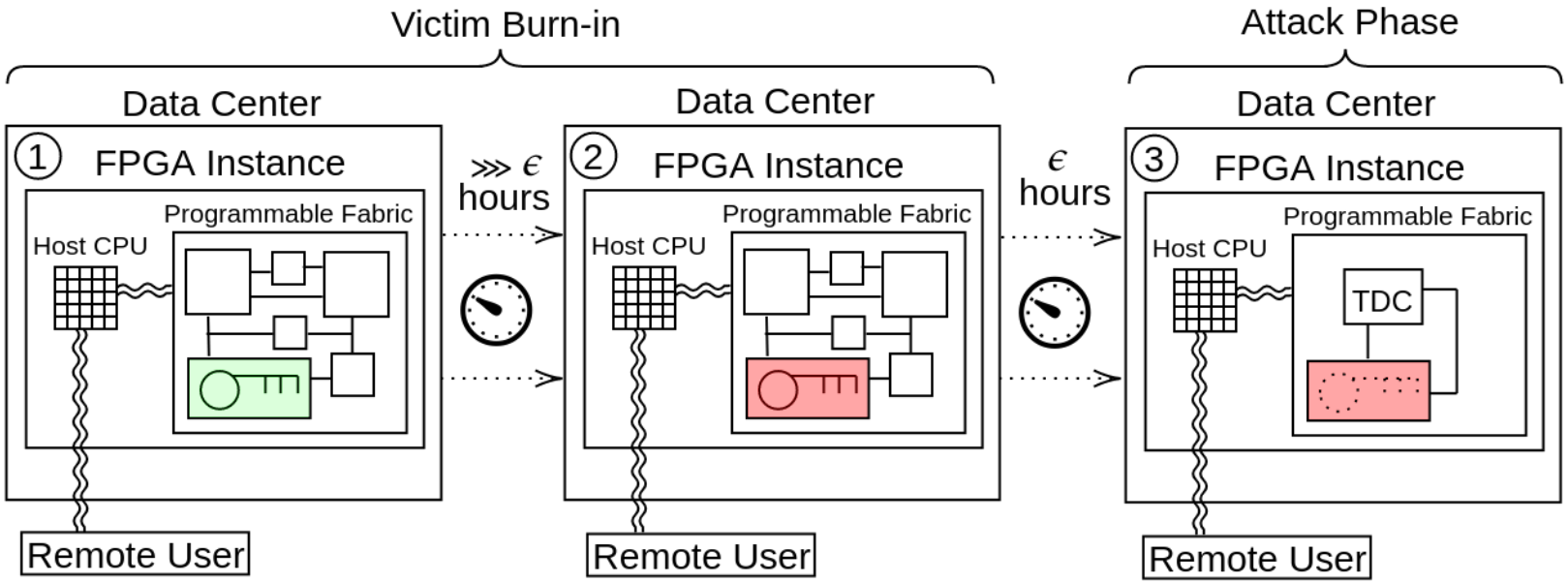

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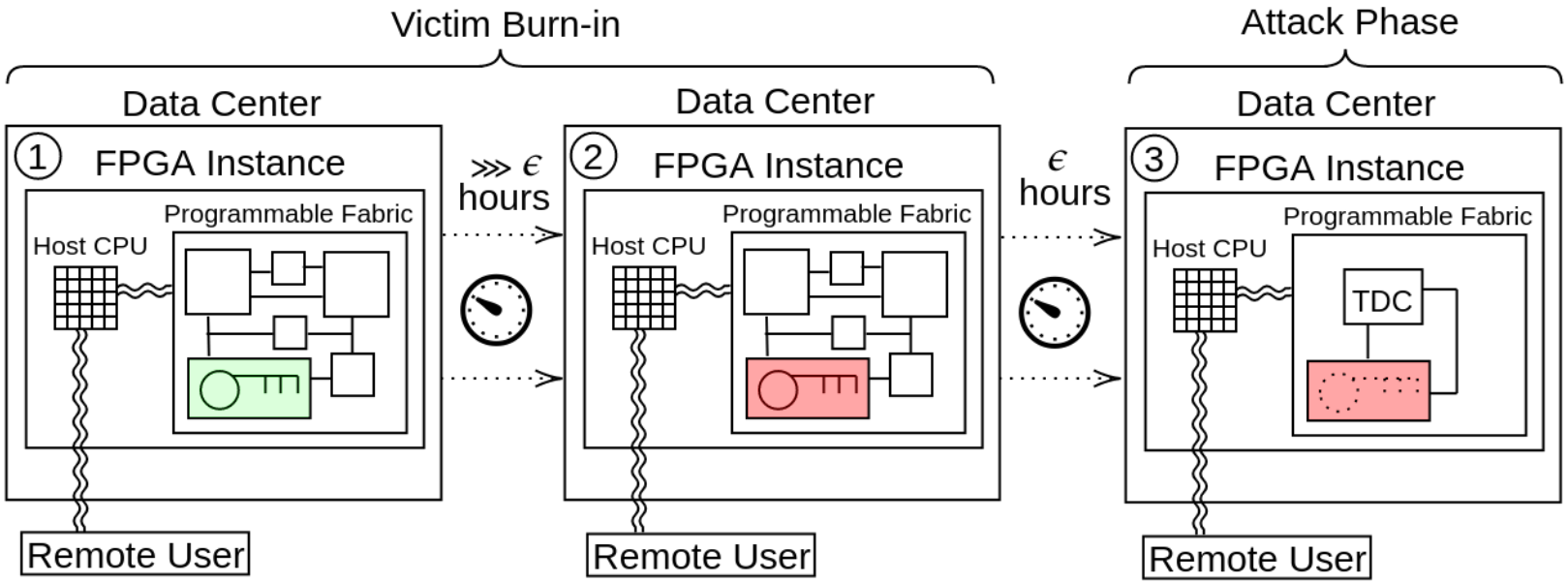

- User rents cloud-FPGA and performs computation using some sensitive data
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- Measures routing which contained sensitive data

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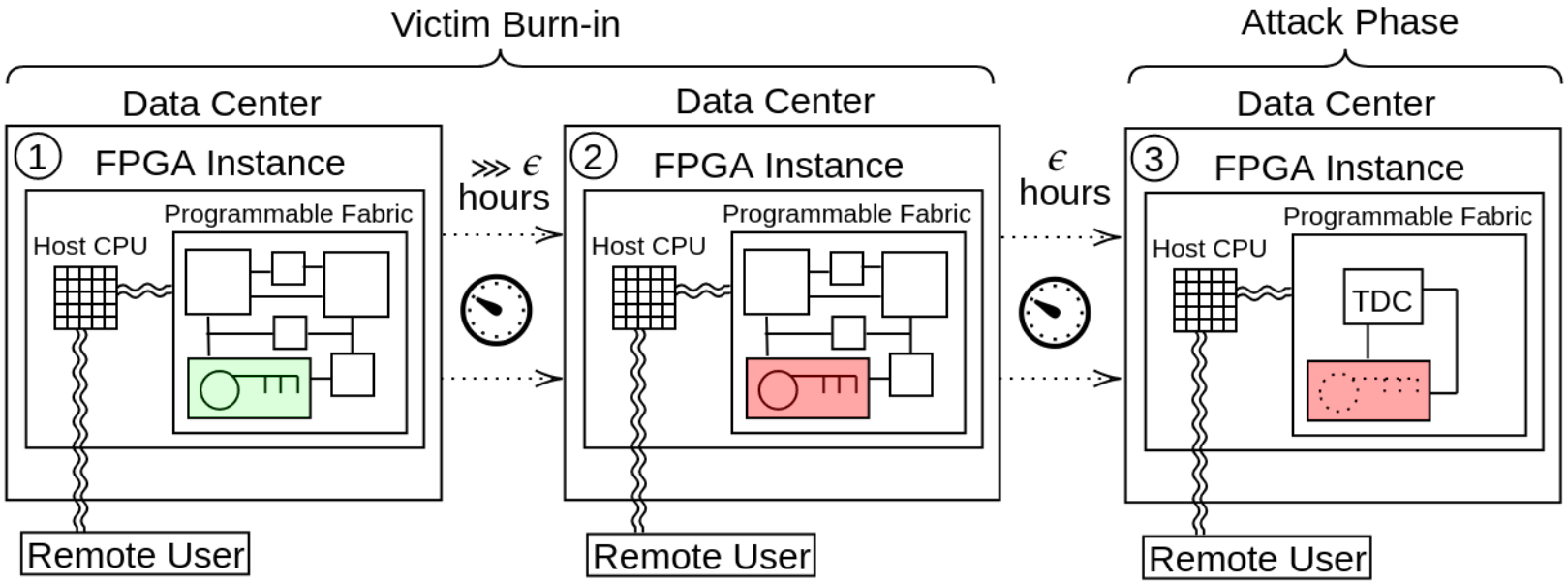

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- Compute....
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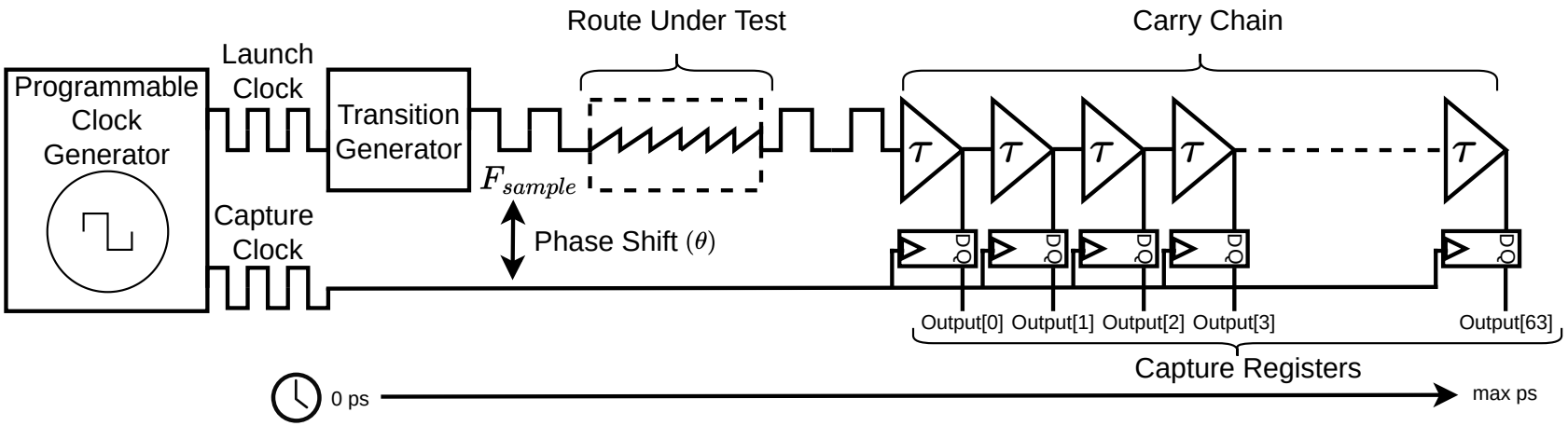
- Measures routing which contained sensitive data
- Extract sensitive data

A Totally Legal, No-Contact Sensor



Output Sequence

Rising Transition 0: 1111_1111_1111_1111_1111_1111_1111_1111_1111_1110_0000_0000_0000_0000_0000_0000

Falling Transition 0: 0000_0000_0000_0000_0000_0110_1111_1111_1111_1111_1111_1111_1111_1111_1111_1111

Rising Transition 1: 1111_1111_1111_1111_1111_1111_1111_1111_1111_1001_0000_0000_0000_0000_0000_0000

Falling Transition 1: 0000_0000_0000_0000_0000_1010_1111_1111_1111_1111_1111_1111_1111_1111_1111_1111

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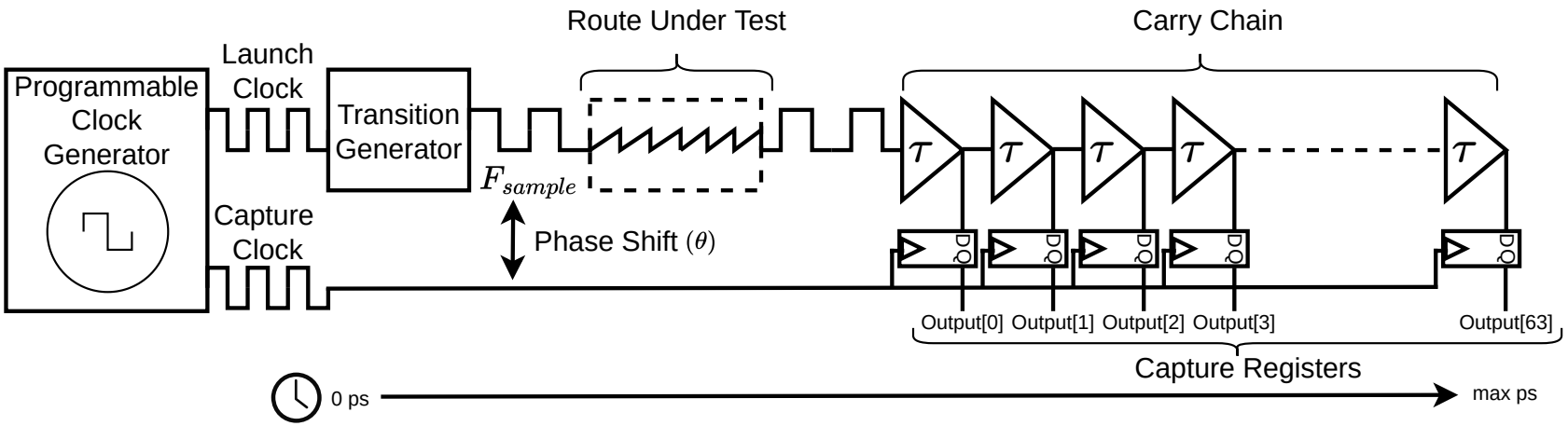

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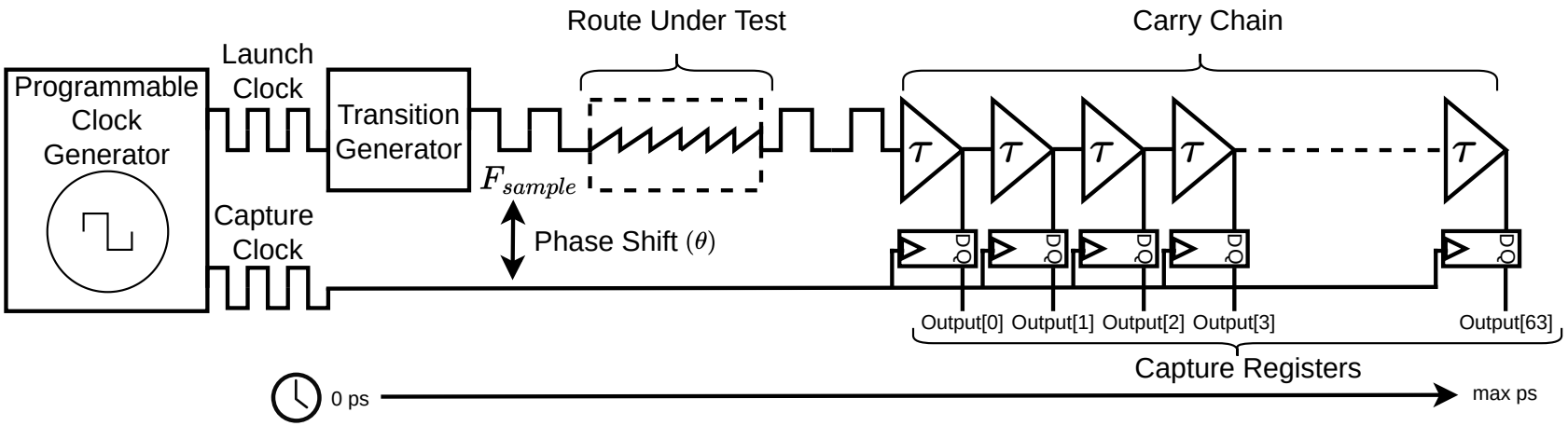
- Undetectable

A Totally Legal, No-Contact Sensor



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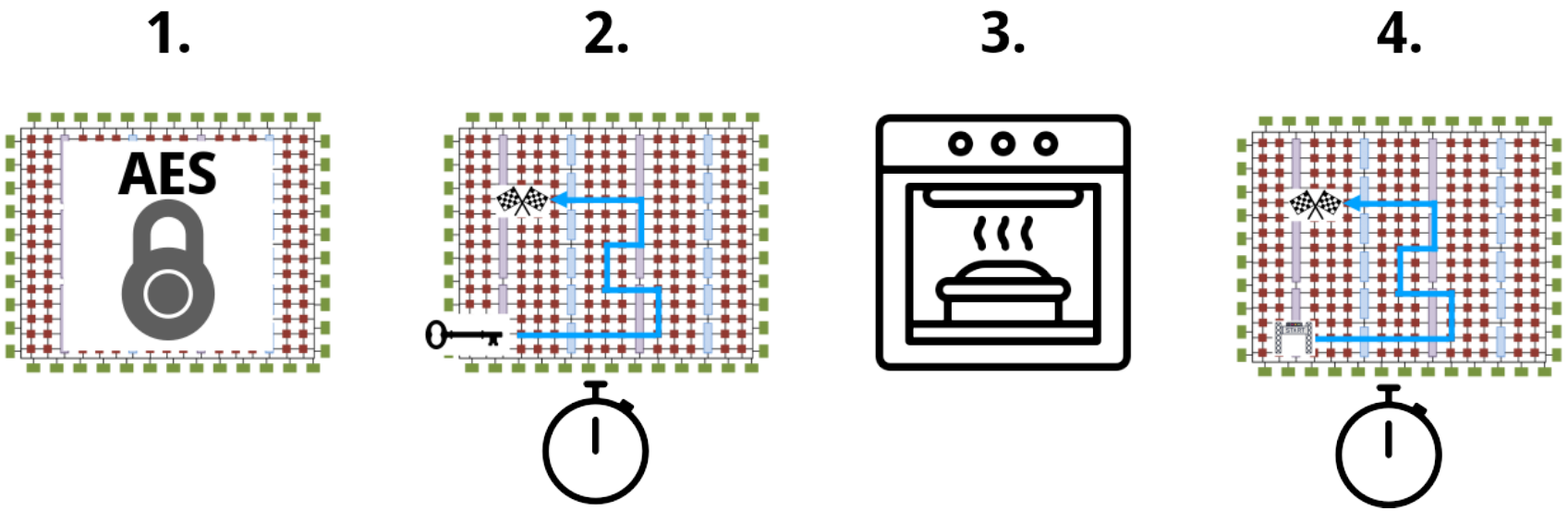
Rising Transition 1: 1111_1111_1111_1111_1111_1111_1111_1111_1111_1001_0000_0000_0000_0000_0000_0000

Falling Transition 1: 0000_0000_0000_0000_0000_1010_1111_1111_1111_1111_1111_1111_1111_1111_1111_1111

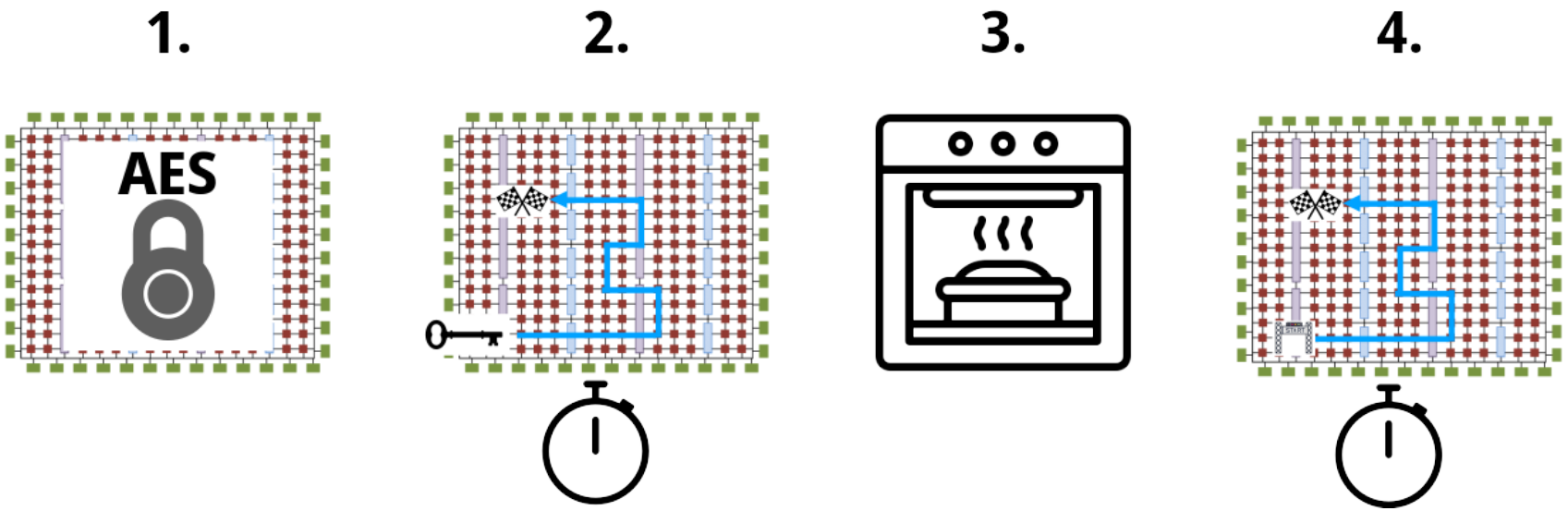
- Undetectable
- Measures timing delay through routing

Experimental Validation



- Instantiate a core that has routes which carry sensitive data

Experimental Validation



- Instantiate a core that has routes which carry sensitive data
- Bake

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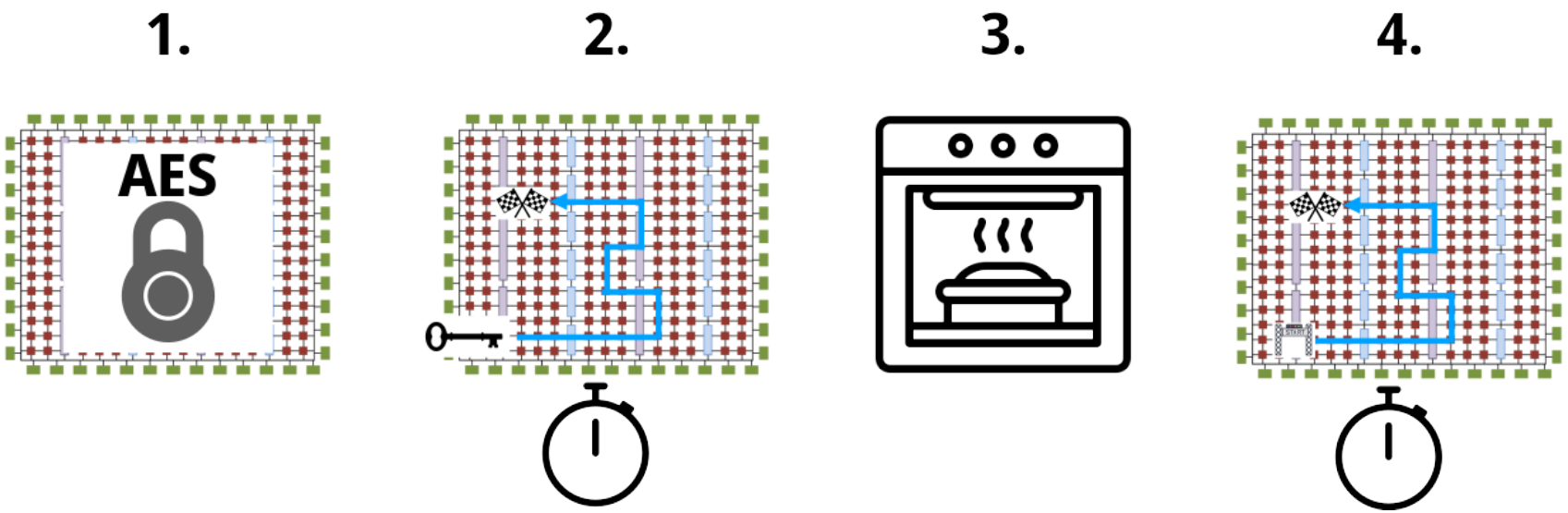
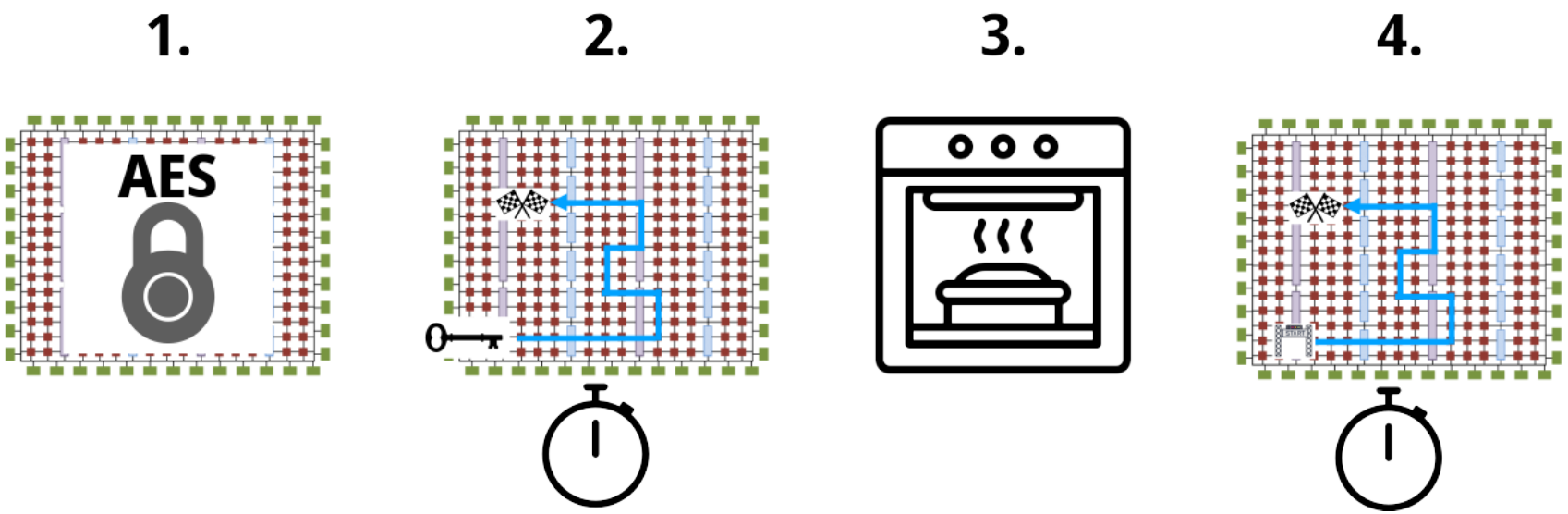


- Instantiate a core that has routes which carry sensitive data
- Bake
- Load design with TDCs and measure delay

Experimental Validation



- Instantiate a core that has routes which carry sensitive data
- Bake
- Load design with TDCs and measure delay
- Repeat

Experimental Results — 10000ps Length Routes

Measure delay of sensitive routes as they bake

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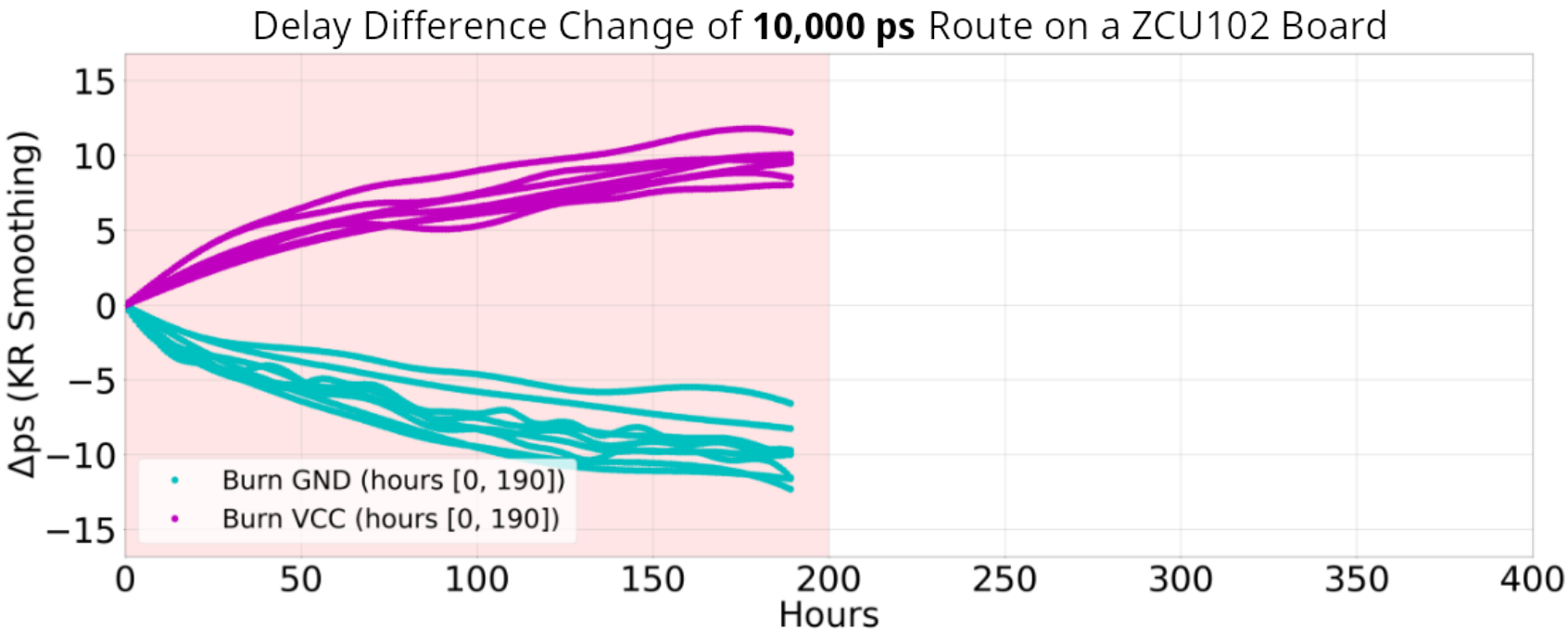

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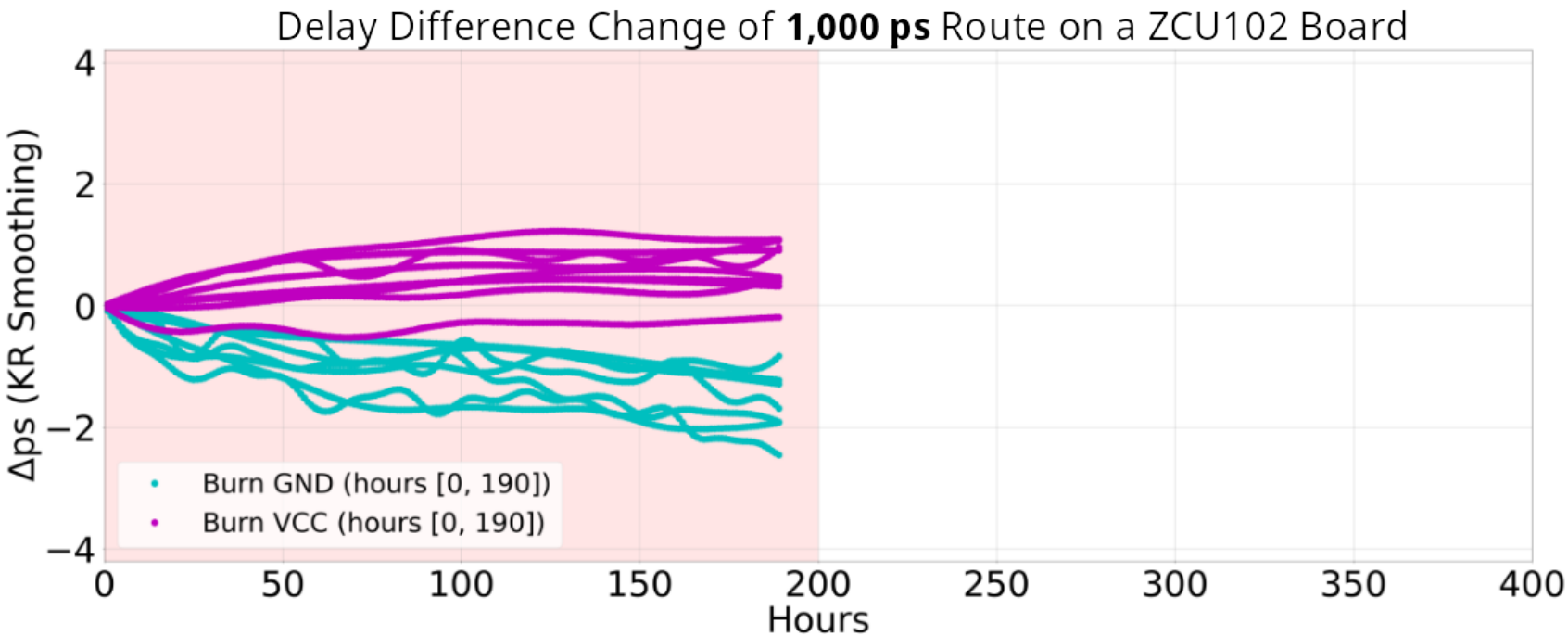
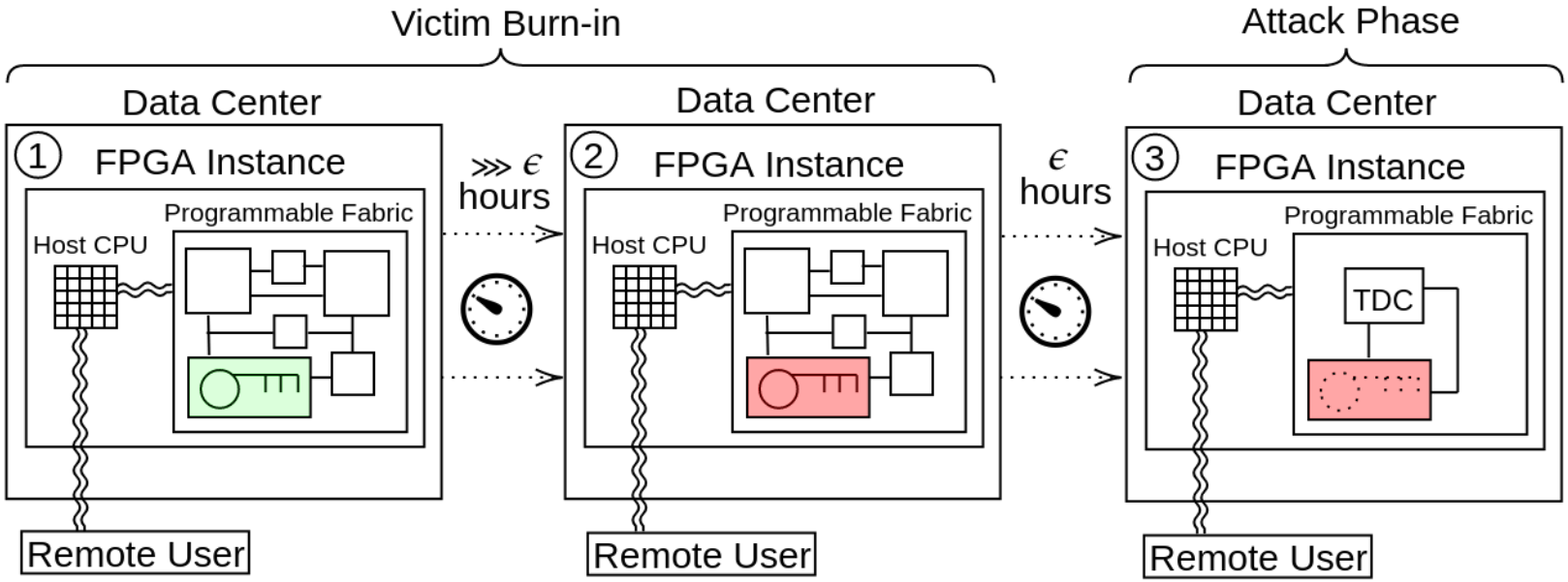


Not Enough For an Attack

If you recall...



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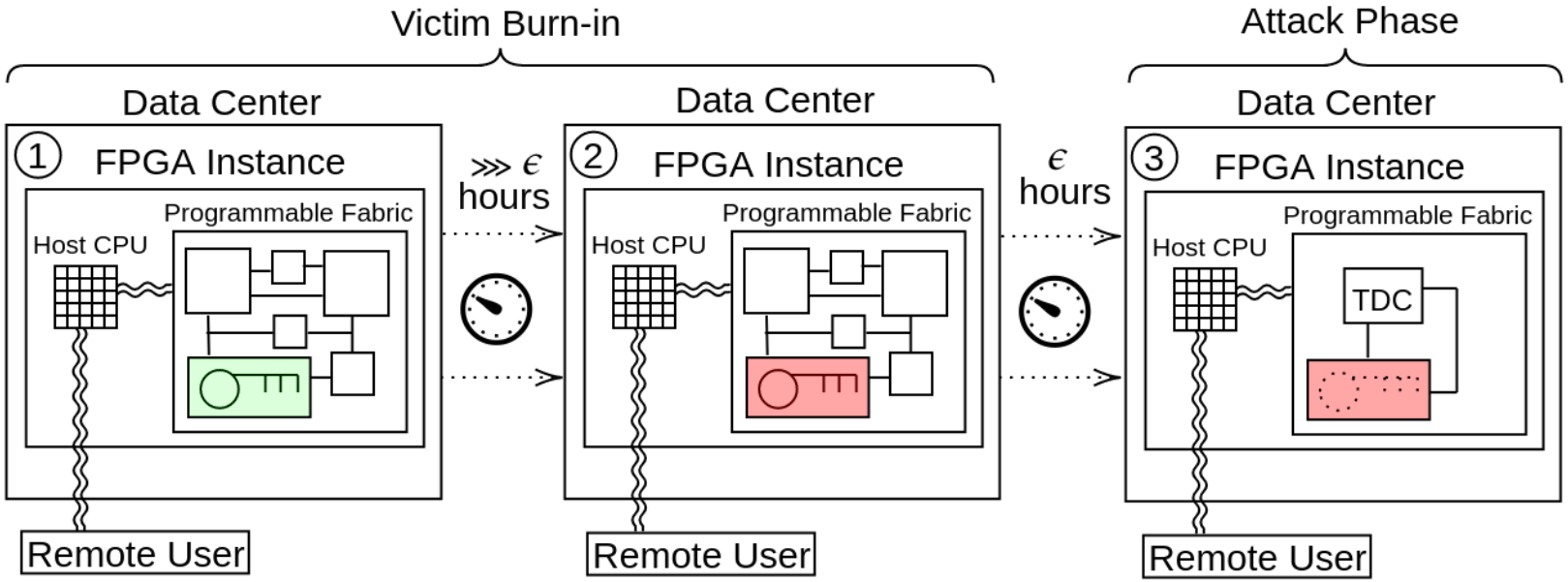

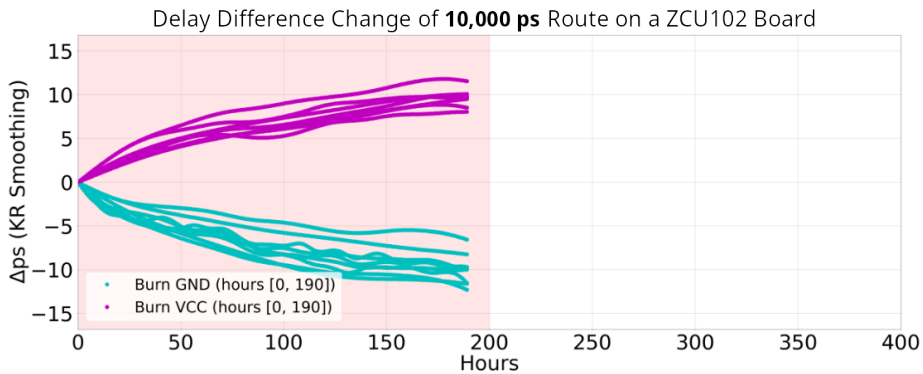

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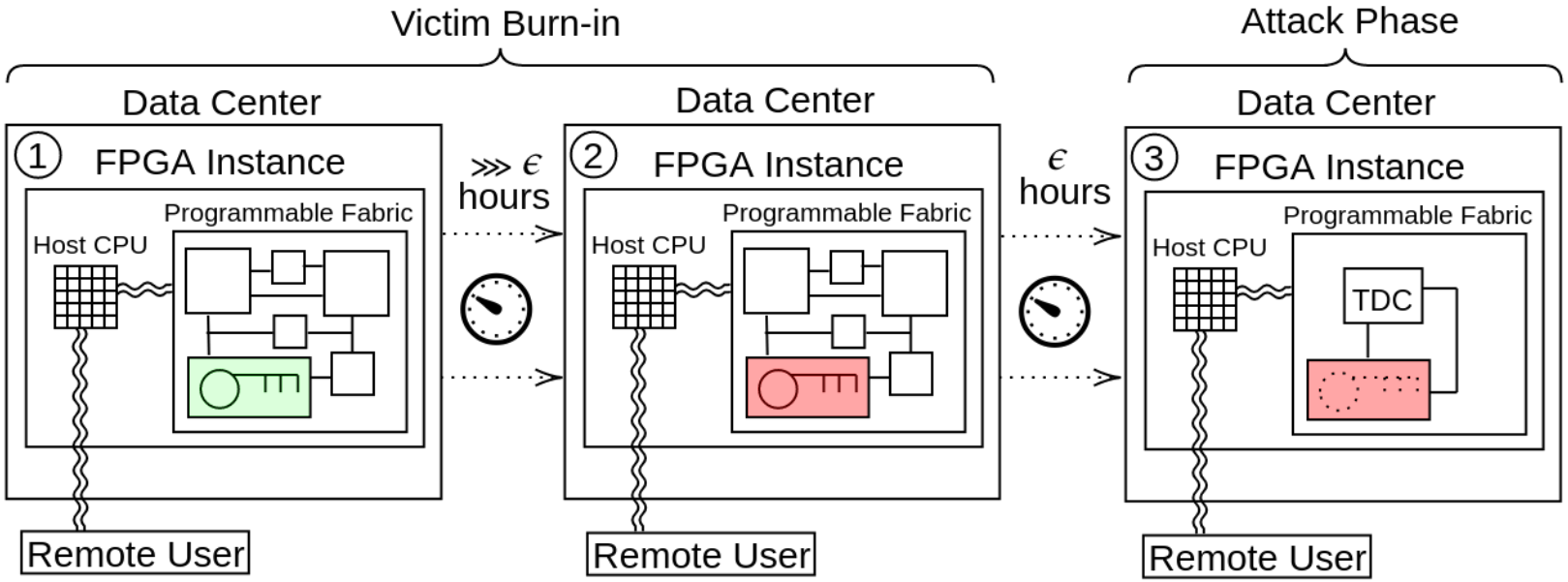

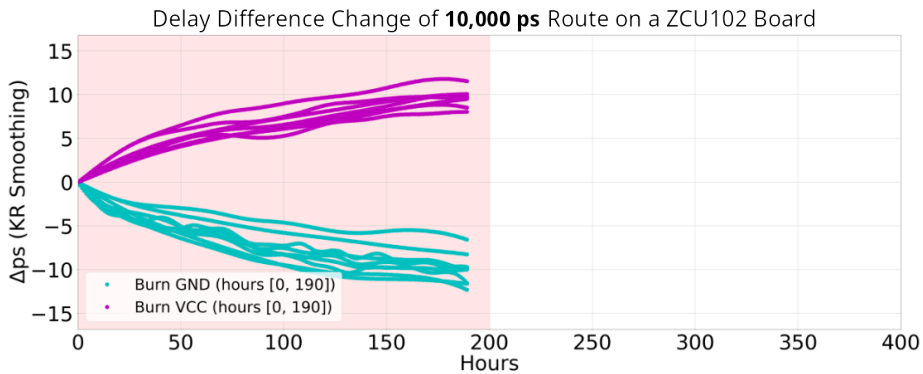

An attacker doesn't know what nominal timing behavior is

An Elastic Effect

Invert the value in sensitive routes

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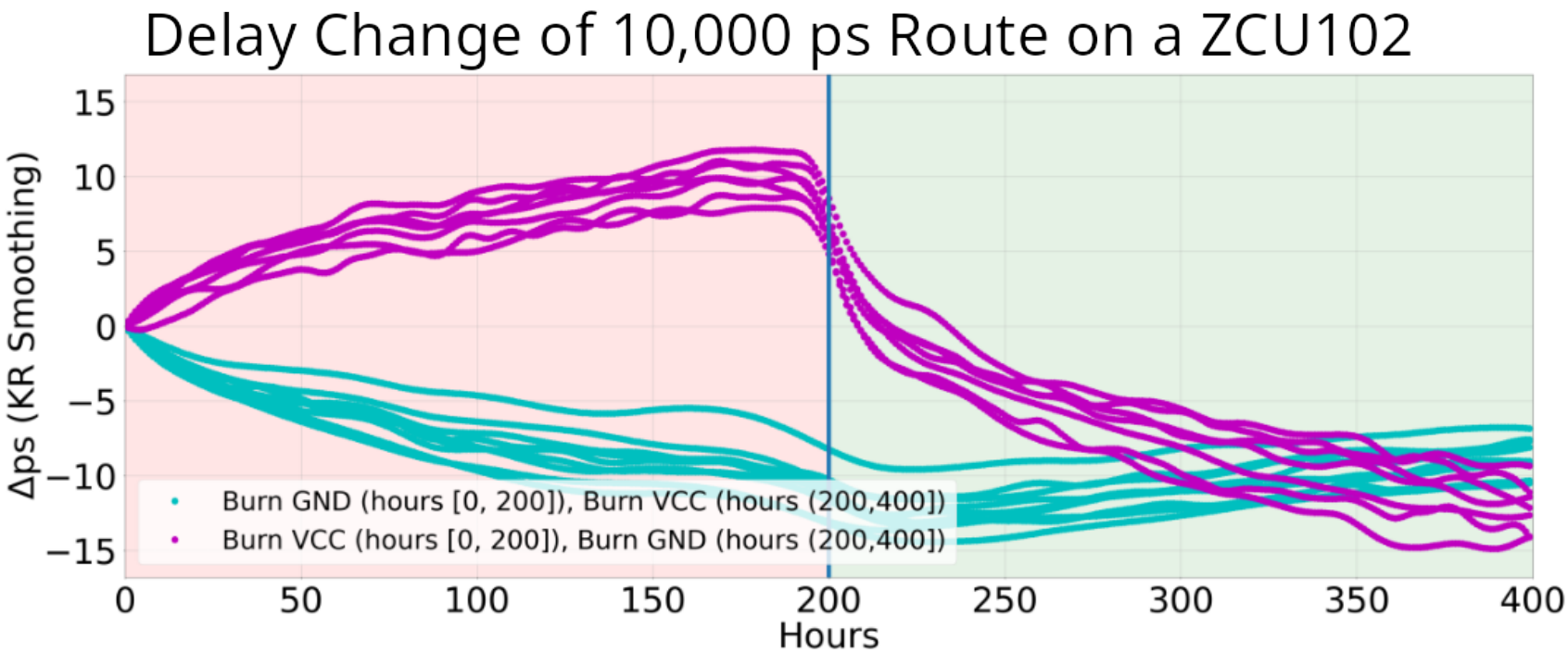

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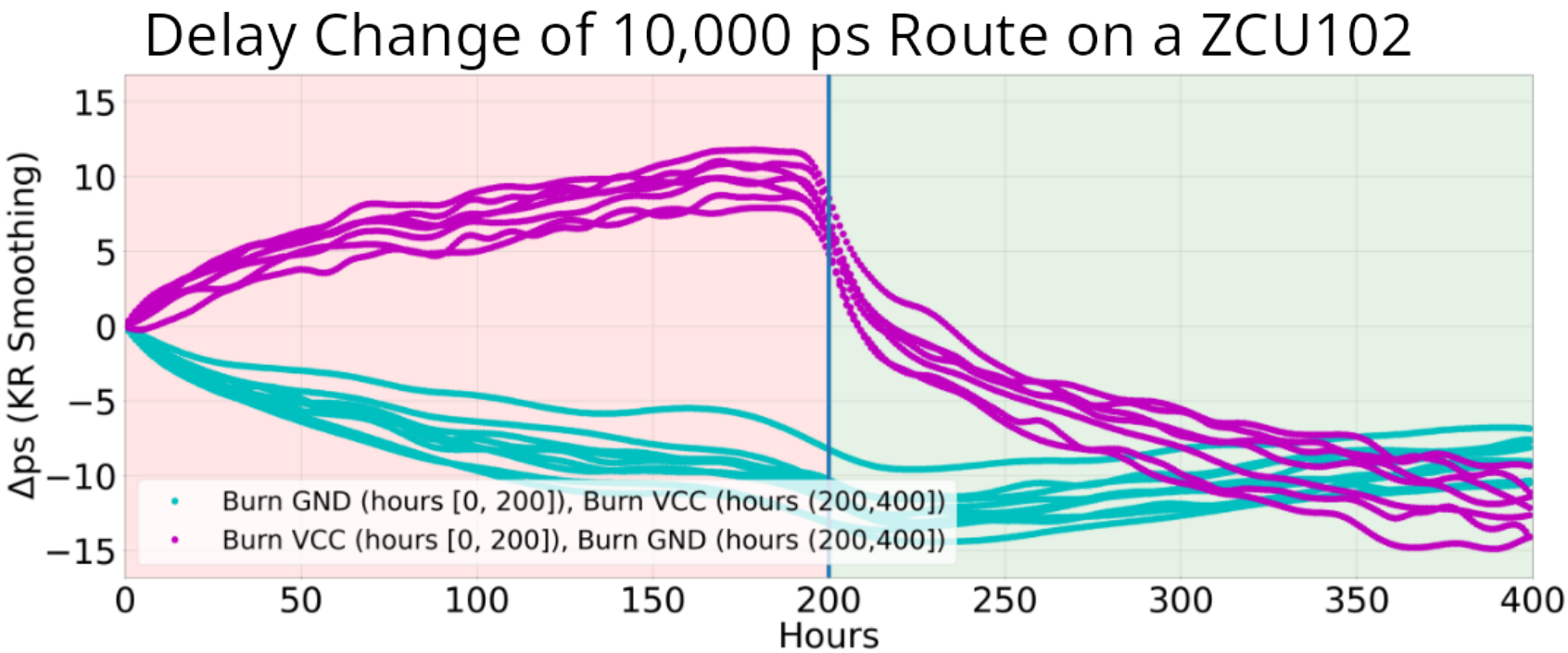
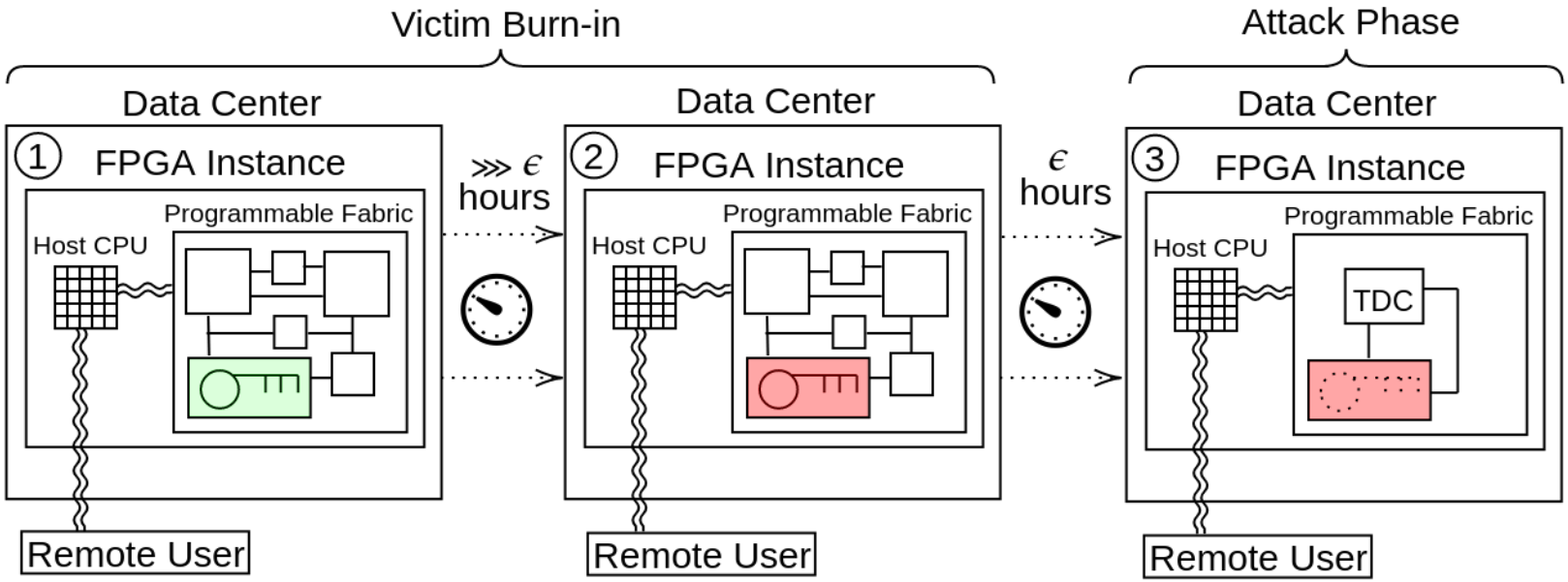


Attacker can apply GND to all routes, study the recovery, and recover original value.

Turning Towards the Cloud...



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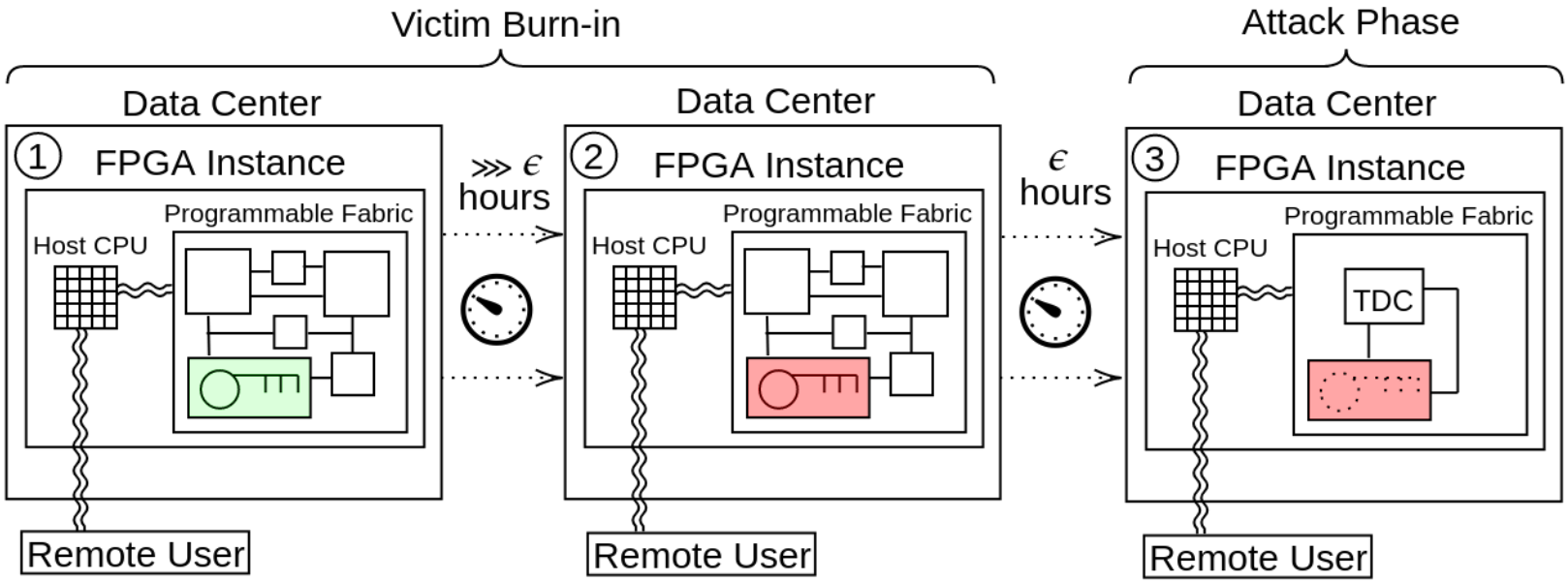

Thanks